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PERFORMANCE ANALYSIS OF CARRY SKIP ADDER USING CNTFET AND FINFET

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Abstract— In this paper, Carry Skip Adder is segregated into many blocks like 1-bit Full Adder, AND gate and MUX. In the place of 1-bit full adder different Full adders using 20T, 16T, 14T, 10T, 9T, and 8T are replaced and analyzed. Propagation delay, Static and dynamic power are the major parameters considered while designing the adders. The results show that the time taken is less in carry propagation over successive stages. Due to less transistor count, Carry Skip Adder has less area, less delay and low power dissipation compared to other adders. The performance analysis is done in CMOS, FinFET and CNTFET in 20nm technology with supply voltage of 0.9v and simulation is done by using Synopsys HSPICE tool.

Keywords— Carry Skip Adder, CNTFET, FinFET, CMOS, HSPICE tool.

I. INTRODUCTION

The major element in many circuits is the significance of low power and high speed adder circuits. Adders are very significant component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Power, Delay and area are the major terms used in this project. Power can be reduced by using different full adders, in Carry Skip Adder. Transistors are scaled down to lower the power dissipation, area and delay.

In this project, Carry Skip Adder circuit using different Full Adders with CMOS, FinFET and CNTFET has done and analysed and its propagation delay, static and dynamic power consumption were analysed and taken. The circuit is simulated using synopsys HSPICE at 20nm technology with supply voltage of 0.9v. This paper is organized as follows Section-II and Section III presents the introduction of CNTFET and FinFET respectively, Section-IV represents about the Adders, Section-V discusses about the Carry Skip Adder, Section-VI shows the Results and Section-VII is done with the conclusion of the paper.

II. THE CARBON NANOTUBE FET

In the fields of nanotechnology, CMOS has supple nature which accounts into many provocations. The main difference between Carbon Nanotube Field Effect Transistor (CNTFET) and MOSFET is that the channel of the devices is formed by CNT's instead of silicon. Which enables a higher drive current density; due to the large current carrier mobility in CNT's compared to bulk silicon. The disadvantage of MOSFET bulks is short channel effect [1]. Due to some manufacturing process and electrical properties CNTFET is one of the desired placement for MOSFET. Carbon nanotubes refers to field Effect Transistor, on the Channel material it uses single Carbon nanotube or an array of carbon nanotubes. By rolling up an extent sized piece of graphite sheet, carbon nanotubes are in the form of hollow sized cylinders. Carbon nanotubes shows semiconducting as well as metallic behaviour based on roll up of graphite sheet during the process [2]. Planar CNTFET is shown in the Fig. 1(a). The metallic and semiconductor tubes existence refers to carbon nanotubes- barrier electronics. The co-axial structure is shown in the Fig. 1(b). Whereas metallic tubes serve as interconnecting wires and active device elements employs as semiconducting tubes. The main emphasis is one dimension in view of electrical properties of carbon nanotubes. This has effective scattering in their systems. The proposed of bulk scattering in case of properties of carbon nanotubes. This has an effective scattering in high conducting carbon nanotubes reduced by decreasing phase space for scattering events. Ballistic way is followed in case of electrons flow, the leakage is low.

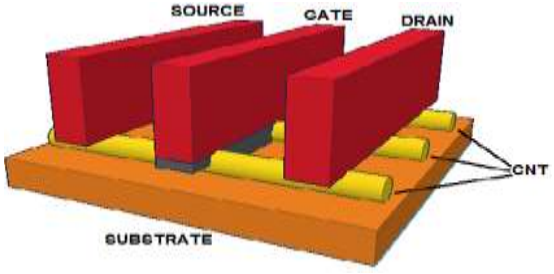

Fig. 1(a) Planar CNTFET

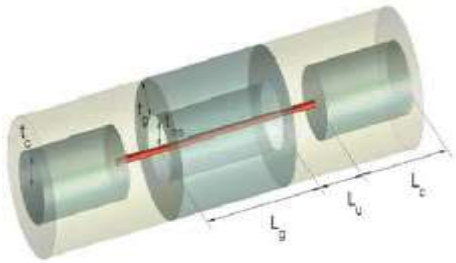

Fig. 1(b) Coaxial structure of CNTFET

III. THE FIN SHAPED FIELD EFFECT TRANSISTOR

The Fin Shaped Field Effect Transistor (FinFET) is a kind of non-planar or 3-Dimensional transistor, it incorporate in an SOI substrate. Above, the insulator FinFET design uses a conducting channel forming a thin silicon structure called gate electrode. Double gate FinFET device is shown in the Fig. 2. FinFET cause into account to overcome the drawback of short channel effect [3]. FinFET application learned on scaled SRAM and analog circuits. Due to difficult gate patterning in the structure high access resistance and doping etc.., many provocations are required for FinFET production. By Optimization of Junction, high resistance is reduced.

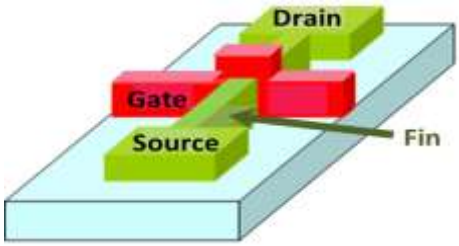

Fig. 2 Double gate FinFET device

IV. ADDERS

A Full Adder is a digital circuit that implements addition of two binary numbers along with the carry input. The Boolean Equations of a Full Adder is given in eq.1 and eq.2.

$$Sum = A \oplus B \oplus C_{in} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$C_{out} = (A \oplus B).C_{in} + A.B \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

This paper presents different full adders with 20 Transistors, 16 Transistors, 14 Transistors, 10 Transistors, 9 Transistors and 8 Transistors by using CMOS, FinFET and CNTFET.

A. 20T Full Adder

(i) 20T CNTFET Full Adder

A 1-bit 20T CNTFET full adder shown in Fig. 3 is also known as Transmission Gate Full Adder (TGA). It consists of CNTFET's, Transmission gates and Inverters. It sustains full output voltage swing which implies this adder has good driving capability.

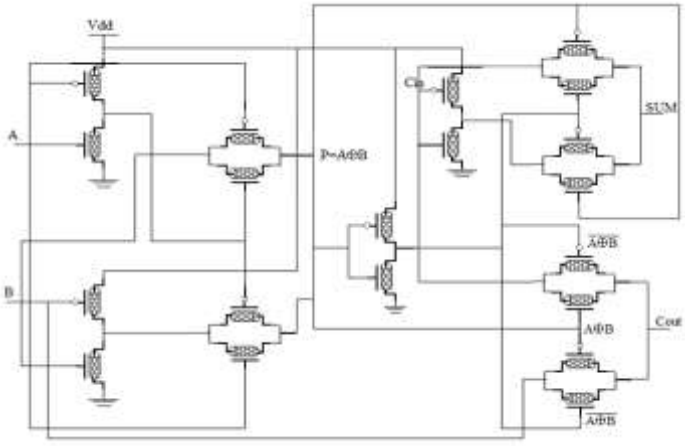

Fig. 3 20T CNTFET Full Adder

(ii) 20T FinFET Full Adder

The 1-bit 20T FinFET full adder shown in Fig. 4. It consists of FinFET's, Transmission gates and Inverters. TGA maintains full output voltage swing.

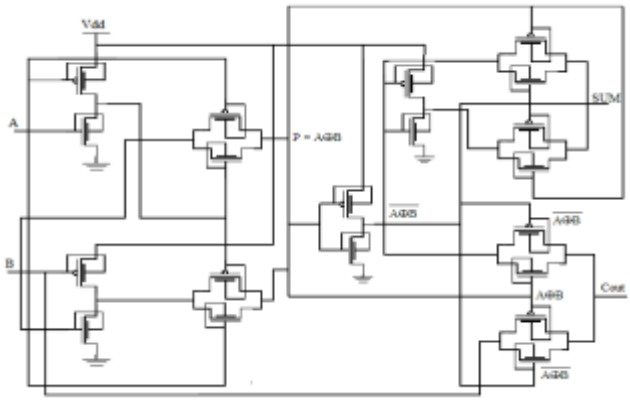

Fig. 4 20T FinFET Full Adder

B. 16T Full Adder

(i) 16T CNTFET Full Adder

A 1-bit 16T CNTFET full adder shown in Fig. 5 is also known as Transmission function adder (TFA). In this circuit there are 2 possible short circuit paths to ground. This circuit uses both pull-up and pull-down logic as well as the complementary pass logic to drive the logic and it consists of CNTFET's, inverters and transmission gates.

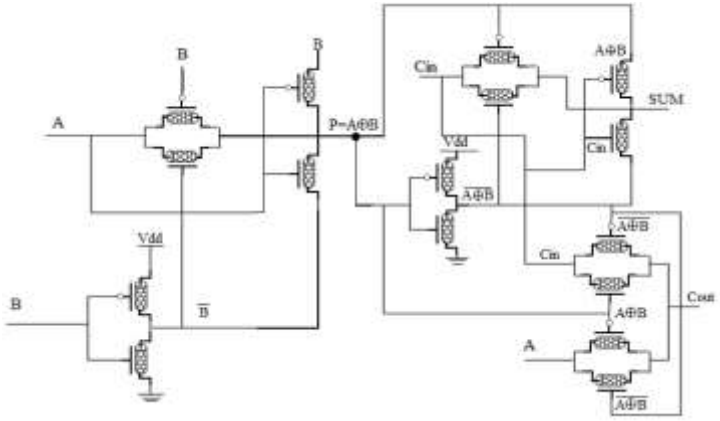

Fig. 5 16T CNTFET Full Adder

(ii) 16T FinFET Full Adder

The 1-bit 16T FinFET full adder shown in Fig. 6. It is improved with FinFET's, inverters and transmission gates and imposes the complementary pass logic to drive the load.

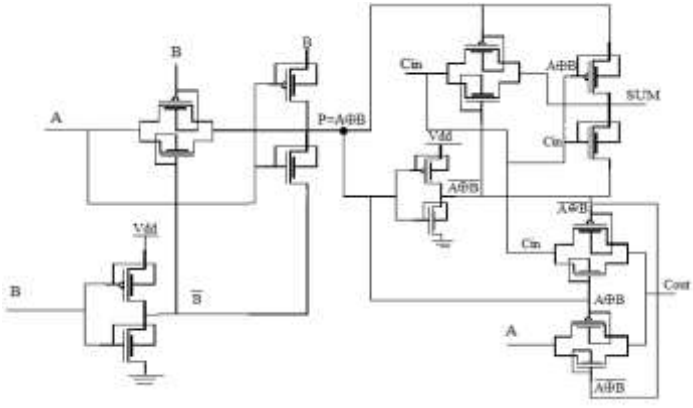

Fig. 6 16T FinFET Full Adder

C. 14T Full Adder

(i) 14T CNTFET Full Adder

A 1-bit CNTFET 14T full adder [4] shown in Fig. 7. It is a combination of Exor gates circuit and a number of transmission gates and pass transistors. It occupies 20% less area than TFA. It implements the complementary pass logic to drive the load.

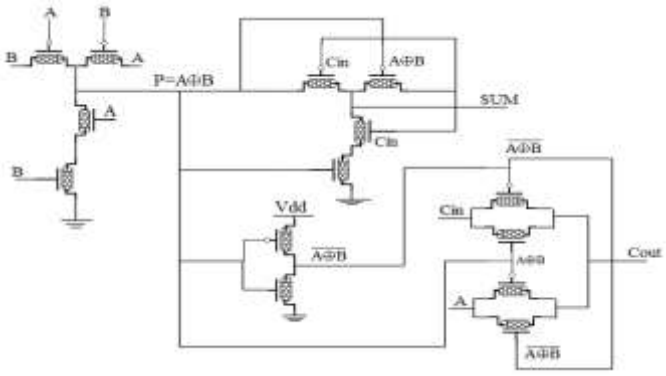

Fig. 7 14T CNTFET Full Adder

(ii) 14T FinFET Full Adder

The 1-bit 14T FinFET full adder is shown in Fig. 8. It is a combination of Exor gates and a number of transmission gates and pass transistors. It implements the complementary pass logic to drive the load.

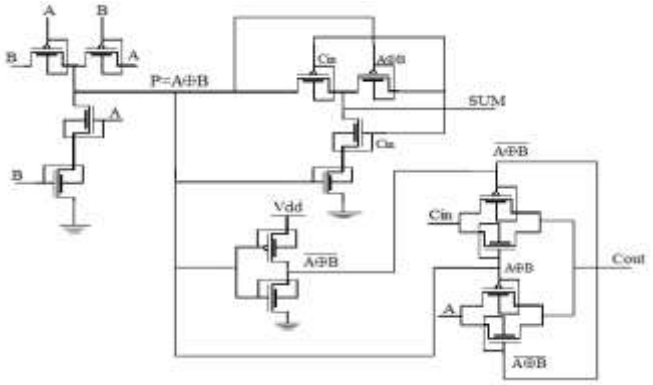

Fig. 8 14T FinFET Full Adder

D. 10T Full Adder

(i) 10T CNTFET Full Adder

A 1-bit CNTFET 10T full adder [5] is shown in Fig. 9. It employs inverters and Pass transistors. This circuit suffers from the lack of driving capabilities in fan-out situation and the performance of it degrades dramatically when they are cascaded. It is having small transistor count and exploits non-full swing.

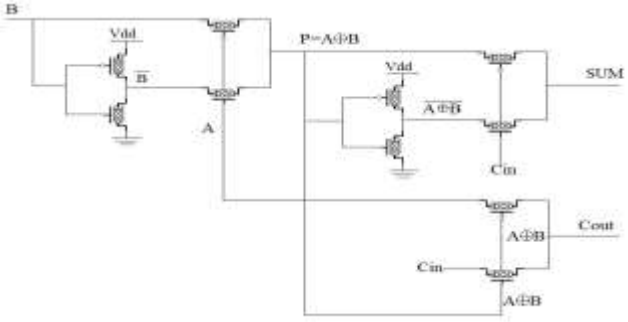

Fig. 9 10T CNTFET Full Adder

(ii) 10T FinFET Full Adder

The 1-bit 10T FinFET full adder is shown in Fig. 10. It consists of inverters and pass transistors. This circuit suffers from the lack of driving capabilities in fan-out situation and the performance of it degrades dramatically when they are cascaded and it maintains non full output swing.

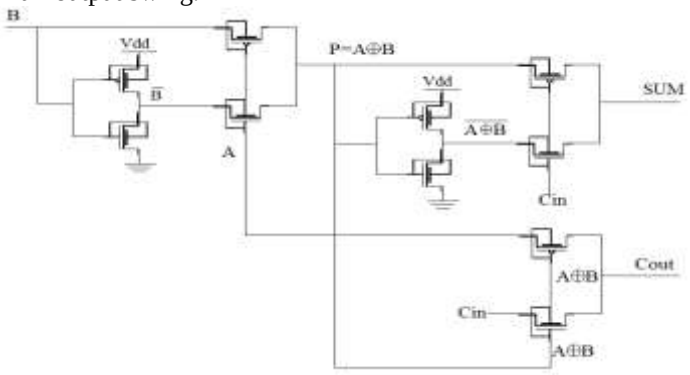

Fig. 10 10T FinFET Full Adder

E. 9T Full Adder

(i) 9T CNTFET Full Adder

A 1-bit 9T CNTFET full adder consists of CNTFET's and pass transistor logics [6]. The 9T CNTFET full adder circuit is shown in Fig. 11. In these pass logic circuits there is usually the power consumption it can realizes complex functions with a minimum of transistors.

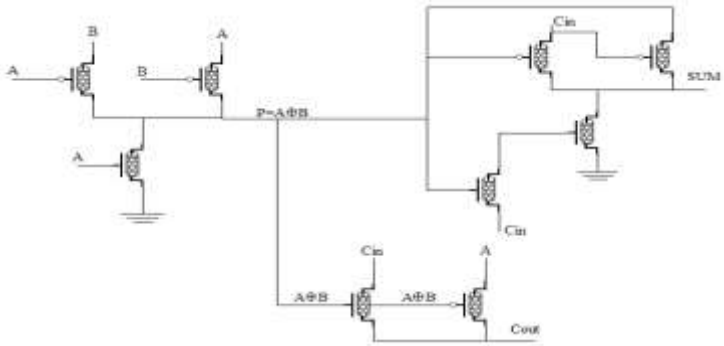

Fig. 11 9T CNTFET Full Adder

(ii) 9T FinFET Full Adder

A 1-bit 9T FinFET full adder is shown in Fig. 12. It consists of FinFET's and pass transistor logics. In pass logic circuit there is usually the power consumption it can realizes complex functions with a minimum of transistors.

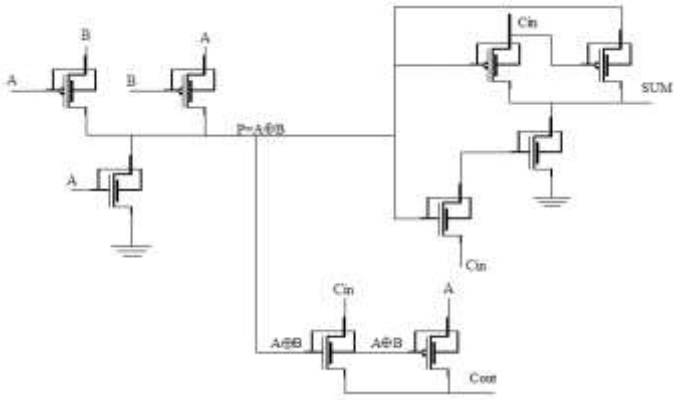

Fig. 12 9T FinFET Full Adder

F. 8T Full Adder

(i) 8T CNTFET Full Adder

A 1-bit 8T CNTFET full adder consists of CNTFET's and pass transistor logics. Fig. 13 shows the 8T CNTFET full adder. It is an essential component of full adder and occupies less area in terms of transistor count [7].

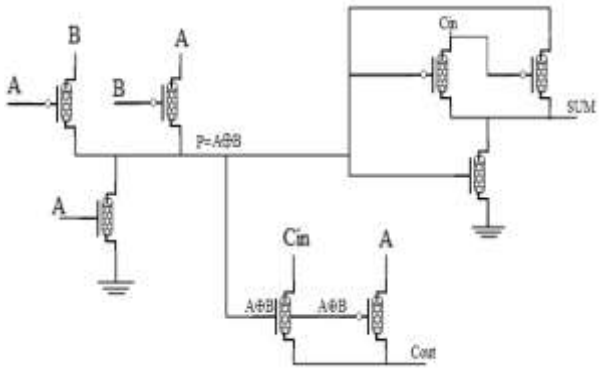

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Fig. 13 8T CNTFET Full Adder

(ii) 8T FinFET Full Adder

The 1-bit 8T FinFET full adder consists of FinFET's and pass transistors. Fig. 14 shows the 8T FinFET full adder. It is a vital component of full adder and occupies less area in terms of transistor count.

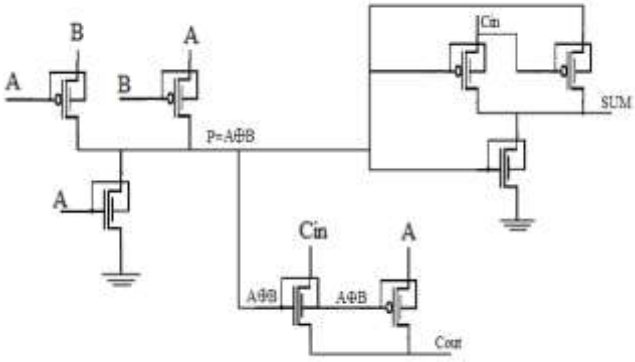

Fig. 14 8T FinFET Full Adder

V. CARRY SKIP ADDER

A Carry Skip Adder (CSKA) is used to reduce the carry propagation time by skipping over group of successive adder stages. A 4-bit CSKA is shown in Fig. 15. Each block has four stages ranging from k to k+3, where, k is the number of the block, from 0 to 3. Each stage consists of a 1-bit Full Adder with two input binary numbers a_i and b_i and the following Boolean equations are given in eq.3, eq.4 and eq.5 where, i is the stage position, P_i is the carry propagation signal, S_i is the sum, C_{i+1} is the carry out and C_i is the carry in for each stage.

$$P_i = A \oplus B \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$S_i = P_i \oplus C_i \quad \ldots\ldots\ldots\ldots\ldots\ldots (4)$$

$$C_{i+1} = A_i \cdot B_i + P_i \cdot C_i \quad \ldots\ldots\ldots\ldots\ldots\ldots (5)$$

The architecture presents CSKA using different full adders like 20T, 16T, 14T, 10T, 9T and 8T. In this CSKA the full adder is replaced with different full adders and performance comparison in terms of static and dynamic power and propagation delay are analyzed using CMOS, FinFET and CNTFET technologies.

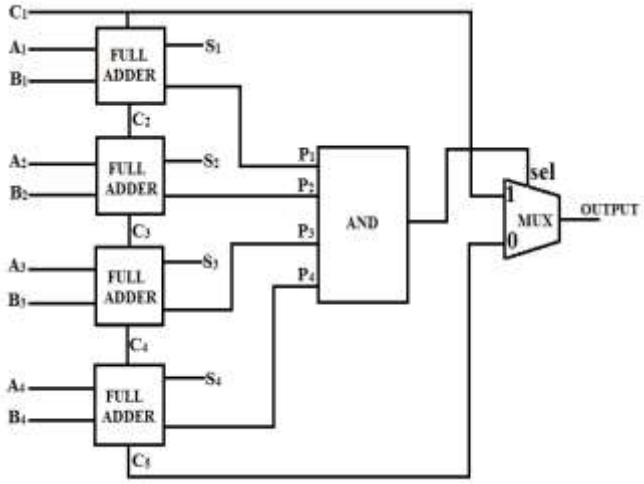

Fig. 15 Block Diagram of a 4-bit Carry Skip Adder

VI. RESULTS

All the CMOS, FinFET and CNTFET full adder circuits and CSKA circuits are designed and simulated using Synopsys HSPICE tool at 20nm technology with 0.9v power supply. Simulation result of full adder is shown in Fig. 16 and CSKA is shown in Fig. 17. Performance Comparison in terms of propagation delay, static power and dynamic power for CMOS, FinFET and CNTFET are tabulated in table I, table II and table III respectively.

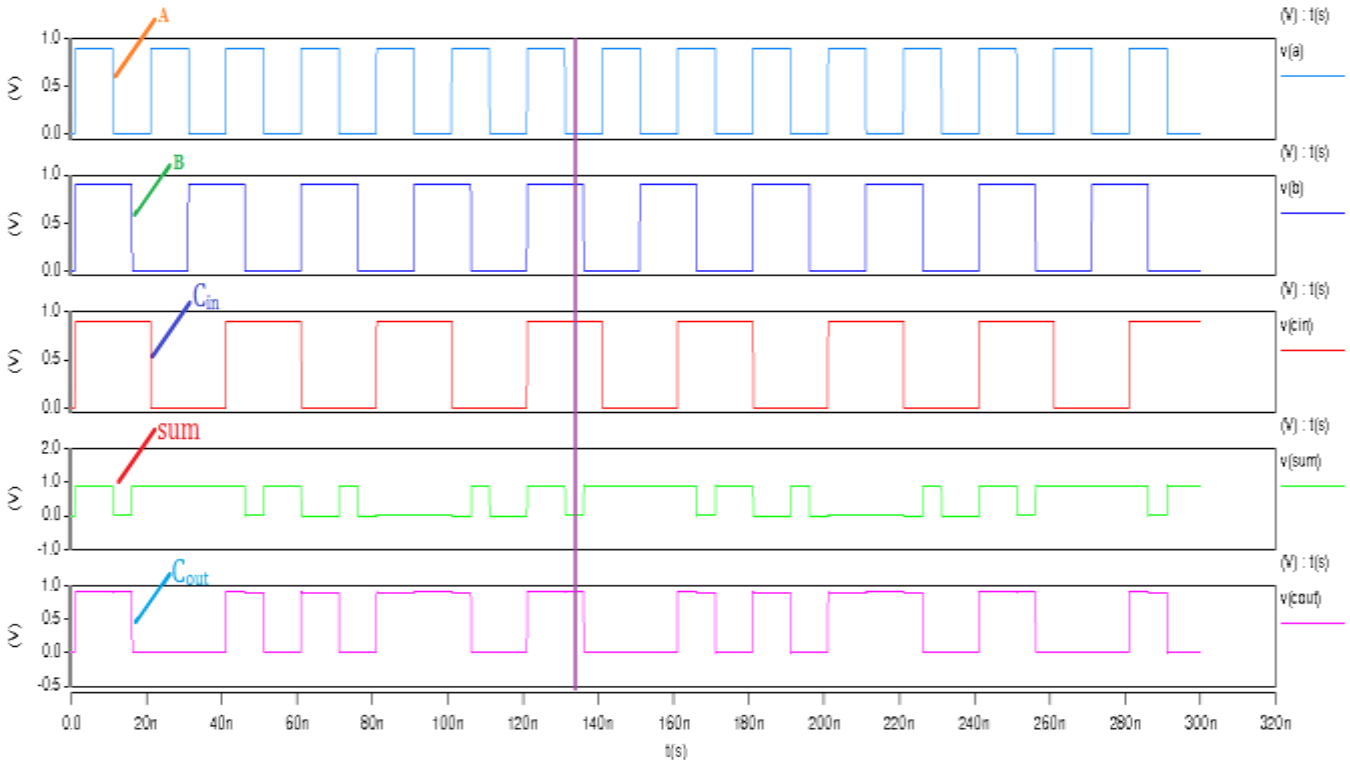

Fig. 16 Full Adder output waveform

From Fig. 16 between 120ns and 140ns the marked input values are A=0, B=C_{in}=1 then from the eq.1 generated sum=0 and from eq.2 C_{out}=1.

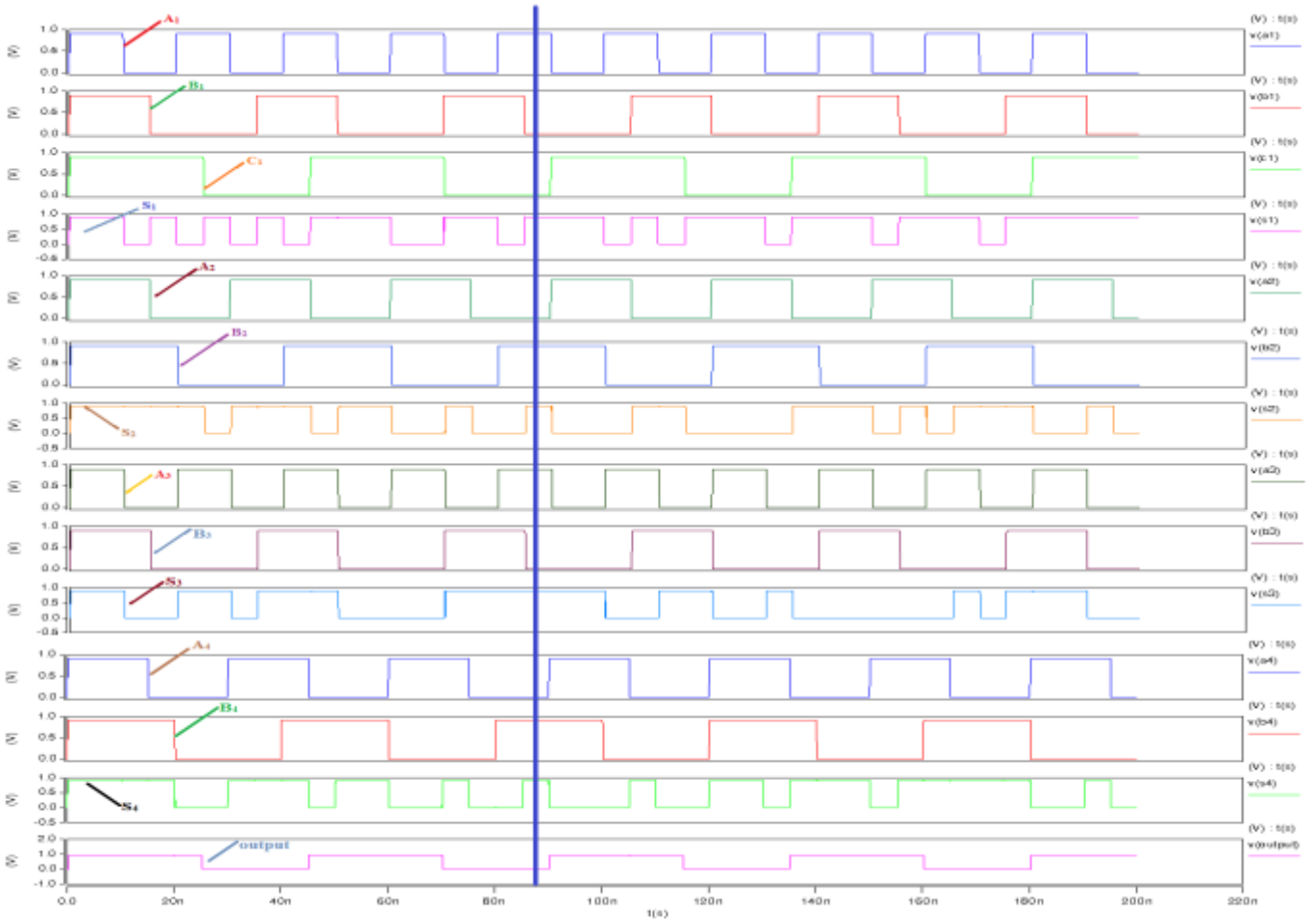

Fig. 17 Output waveforms of Carry Skip Adder

From Fig.17 between 80ns and 100ns if $A_4A_3A_2A_1$=0101 and $B_4B_3B_2B_1$=1010 by performing addition operation we get C_5 value 0. By using eq.3 we get $P_4P_3P_2P_1$=1111 from this 4-input AND gate we get the selection line as 1. Selection line of MUX selects either of the input depending on the output of 4-input AND gate. The output of AND gate is 1, C_1 will be selected.

TABLE I
PERFORMANCE COMPARISION FOR PROPAGATION DELAY

PROPAGATION DELAY	**CMOS (Nano Sec)**	**FinFET (Nano Sec)**	**CNTFET (Nano Sec)**
CSKA using 20 Transistor full adder	0.09	0.01	0.008
CSKA using 16 Transistor full adder	0.08	0.02	0.009
CSKA using 14 Transistor full adder	19.5	0.02	0.020
CSKA using 10 Transistor full adder	0.24	0.15	0.041
CSKA using 9 Transistor full adder	0.46	0.16	0.037
CSKA using 8 Transistor full adder	0.21	0.17	0.037

TABLE II
PERFORMANCE COMPARISION FOR STATIC POWER DISSIPATION

STATIC POWER	**CMOS (Femto Watts)**	**FinFET (Femto Watts)**	**CNTFET (Femto Watts)**
CSKA using 20 Transistor full adder	134.47	122.55	4.30
CSKA using 16 Transistor full adder	70.61	7.17	0.75
CSKA using 14 Transistor full adder	27.52	3.20	0.92
CSKA using 10 Transistor full adder	19.55	17.70	0.92
CSKA using 9 Transistor full adder	524.05	17.75	1.00
CSKA using 8 Transistor full adder	542.61	190.08	0.94

TABLE III
PERFORMANCE COMPARISION FOR DYNAMIC POWER DISSIPATION

DYNAMIC POWER	**CMOS (Micro Watts)**	**FinFET (Micro Watts)**	**CNTFET (Micro Watts)**
CSKA using 20 Transistor full adder	6.72	6.12	0.21
CSKA using 16 Transistor full adder	3.53	0.35	0.03
CSKA using 14 Transistor full adder	1.37	0.16	0.04
CSKA using 10 Transistor full adder	0.97	0.88	0.04
CSKA using 9 Transistor full adder	26.20	0.88	0.05
CSKA using 8 Transistor full adder	27.13	9.50	0.04

VII. **CONCLUSION**

This paper presents Carry Skip Adder (CSKA) with different full adders like 20T, 16T, 14T, 10T, 9T and 8T using CMOS, FinFET and CNTFET technologies and simulated by using Synopsys HSPICE 20nm technology with 0.9v power supply. Performance results in terms of propagation delay, static and dynamic power of CMOS, FinFET and CNTFET are comparatively analysed. CNTFET CSKA has less static and dynamic power dissipation compared to CMOS and FinFET technologies and also CNTFET CSKA has high speed performance compared to CMOS and FinFET technologies.

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