International Journal of Technical Innovation in Modern Engineering & Science (IJTIMES)
Impact Factor: 5.22 (SJIF-2017), e-ISSN: 2455-2585
Volume 4, Issue 6, June-2018

DESIGN AND DEVELOPMENT OF MULTILEVEL INVERTER TO IMPROVE POWER QUALITY

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Abstract— Multi-level inverters have become an upmarket technology in medium and high power application. This paper presents a cascade H-bridge topology using of bidirectional MOSFET switching control which improves the performance and reliability of multilevel inverter. An experimental study on THD content of proposedCascaded H-bridge multilevel inverter (CHMLI)andconventional UPS is carried out. PWM control scheme is employed to attain synchronised triggering and power frequency stepped output wave.CHMLI utilizes 'n' H-bridgesand dc sourcesto obtain '2n+1' levels of output voltage.Reduction in THD content with improved voltage profile to improve the overall power quality are the main concerns of the proposed scheme in thispaper. Hardware in the loop (HIL) Simulation of CHMLI model is done using Proteus software. A prototype of the proposed seven-level topology is built and tested to analyze the performance of the inverter. This is achieved by examiningthe results of an experiment, which indicated improved power quality and 40% reducedTHD, than 3 level inverter.

Keywords:Cascaded H-bridge multilevel inverter (CHMLI), Total harmonic distortion (THD), Pulse width modulation (PWM), Hardware in the loop (HIL).

I. INTRODUCTION

In the areas of power conversion, an inverter plays a vitalrole. However, increase in use of power electronic based devices leads to unwanted harmonics in the power system which affects the power quality and reduces useful life of equipment. Development in multilevel inverter technologies will become one of the important alternatives in power system. Research is going on to improve performance, optimise control techniques, reduce component count and manufacturing cost. There are several types of topologies which have been developed for multilevel inverter system by manufacturer to increase the number of levels, reduce the count of component, number of independent dc source, voltage stresses and losses. The most commonly used topologies are cascaded H-bridge, flyingcapacitor, diodeclamped.

This paper is organised in the following manner. Section II presents block diagram description of Cascaded H-bridge multilevel inverter, Section III presents circuit configuration and operation mode of CHMLI, Section IV presents the switching strategy, section V includes the experimental results and the conclusion is summarised in section VI.

II.BLOCK DIAGRAM AND DESCRIPTION.

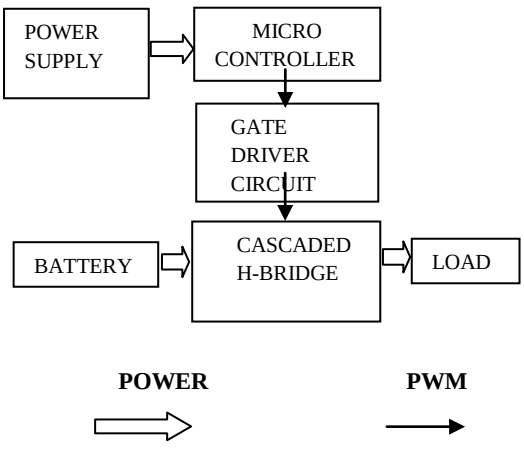


Fig 2.1: Block diagram of CHMLI

Fig 2.1 shows the block diagram of CHMLI.Each cascaded H-bridge is powered by individual battery source. Output of cascaded H-bridges isconnected to a Single phase load. Switching of H-bridges is controlled by microcontroller through gate driver circuit. Gate driver circuit consist of Opto-isolator whichisolates power and control circuit. Synchronized switching strategy obtained by microcontroller to generate stepped output voltage at power frequency.

III. CIRCUIT CONFIGURATION

The main circuit configuration of 7-level CHMLI is shown in fig.3.1. CHMLI requires 'n' H-bridges and 'n' dc sources to get '2n+1' levels at output voltage. Threeseparate dc sources Vdc1, Vdc2 and Vdc3required to get 7 level stepped output.Each H-bridge contains eight power MOS-FET switches (P-channel and N-channel) which denoted by S1, S2, S3,S4, S5, S6, S7 and S8.The CHMLI output is fed to single phase load.

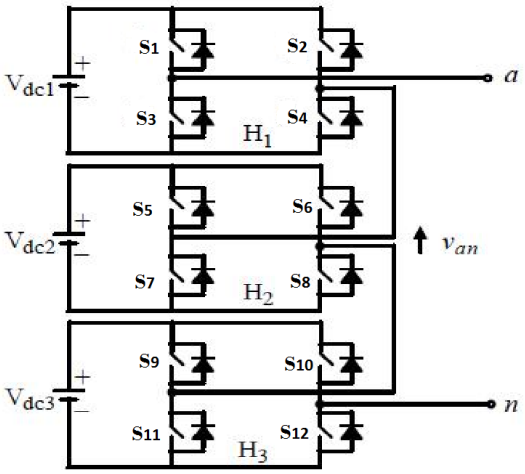


Fig3.1: Single phase 7 level CHMLI.

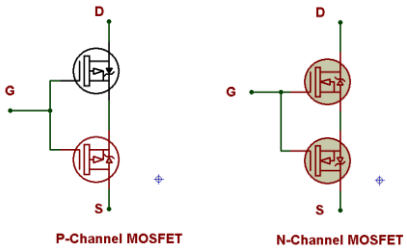


Fig 3.2: Switch Arrangement

[A]: Switch configuration

MOSFET are unipolar device which means only one directional control is achieved, to achieve bidirectional control unique MOSFET switching arrangement is used as shown in fig 3.2. Switch S1, S2, S5, S6, S9, S10 are P-channel MOSFET and S3, S4, S7, S8, S11, S12are N-channel MOSFET.

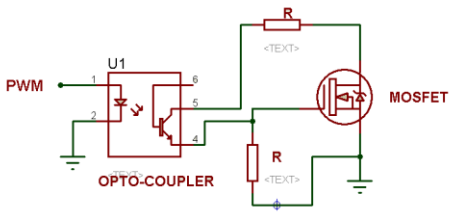


Fig 3.2.1: Switch Arrangement

[B] Control circuit configuration

Opto-couplers are used to drive gate as well as provide isolation between power and control circuit as shown in fig 3.2.1. A unique arrangement of resistor and transistor help to drive MOSFET at low power andfast switching is achieved.

Fig 3.3 shows detailed output voltage waveform of single phase CHMLI.There are seven level of output voltage waveform consist of 0, +Vdc, +2Vdc, +3Vdc, -Vdc,-2Vdc, -3Vdc. Tis the total time period.

The three H-bridge circuit are connected in series in such manner that synthesized total output voltage waveform is the sum of three individual H-bridge circuit output.

Total output voltage is,

Vo (AC)= (Vdc+ Vdc+ Vdc)/√2 =3Vdc/√2

Where,

Vo(AC)=load voltage.

Vdc= H-Bridge DC source voltage

IV. SWITCHING STATERGY

There are total seven different mode of operation of single phase seven level CHMLI. There are seven levels of outputvoltage waveform as shown in fig 3.3.

Table1: Switching Pattern for 7 level CHMLI

MODE	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	Angle	Voltage
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	θ0	0
1	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	θ1, θ2'	Vd1
2	ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	ON	θ2, θ3'	Vd2
3	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	θ3	Vd3
4	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	- θ1 , - θ2'	-Vd1
5	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	- θ2, - θ3'	-Vd2
6	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	-θ3	-Vd3

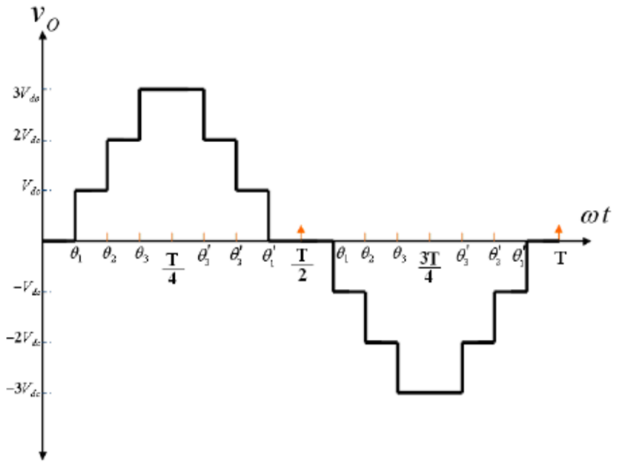


Fig 3.3: output voltage waveform of single

For seven different modes of operation switching sequence is shown in table 1 each mode of operation explained below.

Mode 0:

In mode 0, switches S1 to S8 are turned OFF. Dc voltage Source is not connected to load.

Output voltage is zero.

Mode 1:

In mode 1, switch S1, S4, S7, S8, S11 and S12 are turned ON at angle θ1. Dc voltage Source is connected to load. Output voltage across the load is +Vd1.Same pattern is turned on again at θ2'.

Mode 2:

In mode 2, switches S1, S4, S5, S8, S11 and S12 are turned ON at angle θ2. Dc voltage Source is connected to load. Output voltage across the load is +Vd2.Same pattern is turned on again at θ3'.

Mode 3:

In mode 3, switches S1, S4, S5, S8, S9 and S12 are turned ON at angle θ3. Dc voltage Source is connected to load. Output voltage across the load is +Vd3.

Mode 4:

In mode 1, switch S2, S3, S5, S6, S9 and S10 are turned ON at angle -θ1. Dc voltage Source is connected to load. Output voltage across the load is -Vd1.Same pattern is turned on again at -θ2'.

Mode 5:

In mode 2, switches S2, S3, S6, S7, S9 and S10 are turned ON at angle -θ2. Dc voltage Source is connected to load. Output voltage across the load is +\-Vd2.Same pattern is turned on again at -θ3'.

Mode 6:

In mode 3, switches S2, S3, S6, S7, S10 and S11 are turned ON at angle -θ3. Dc voltage Source is connected to load. Output voltage across the load is -Vd3.

V. EXPERIMENTAL RESULT

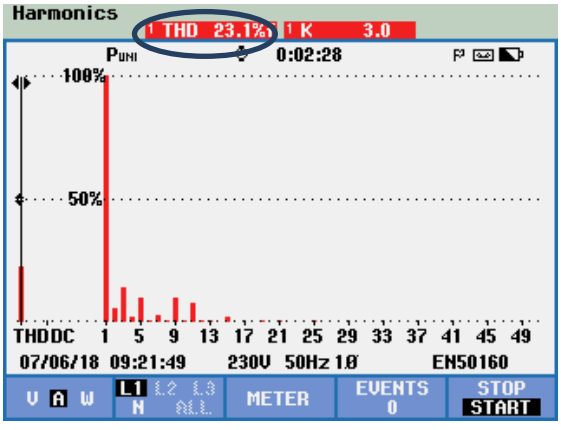
A prototype of CHMLI (7 level) is developed and compared with 3 level inverter and results obtained are summarised in table 2.

A] *THD MEASUREMENT*:

The total harmonic distortion (THD) is a measurement of the harmonic distortion present in an output voltage and current waveform of CHMLI inverter.THD of output waveform of inverter with respect to pure sin wave measured by power quality analyser or THD analyser.

The stepped waveform of CHMLI becomes more sinusoidal as the number of output voltage levels of increases+.In sevenlevelinverter THD is less as compared to three level inverter.

Fig 3.4.1: CHMLI (7 Level) current THD content (Measured by harmonic analyzer).



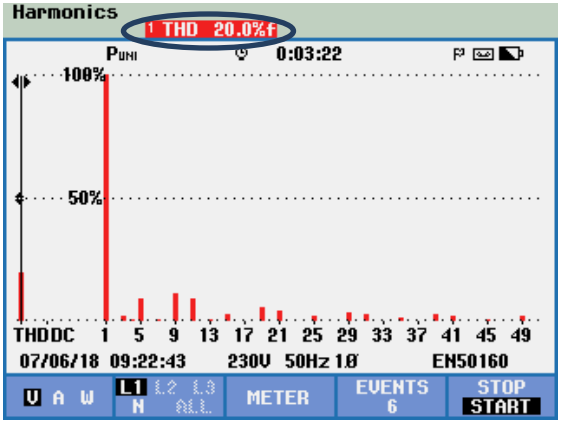


Fig 3.4.2: CHMLI (7 Level) voltage THD content (Measured by harmonic analyzer).

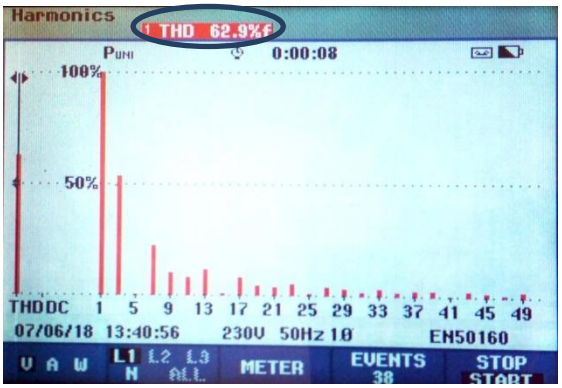


Fig 3.4.3: 3 level inverter voltage THD content (Measured by harmonic analyzer).

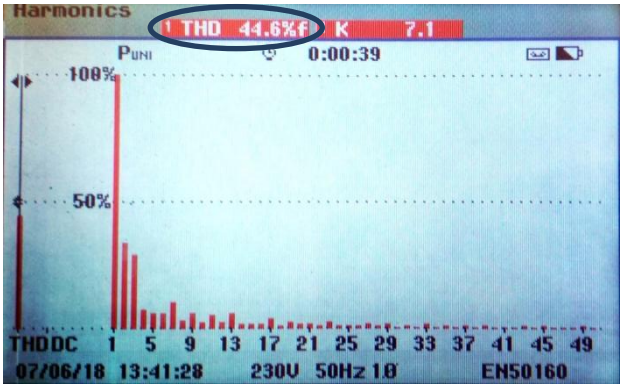


Fig 3.4.4: 3 level inverter current THD content (Measured by harmonic analyzer).

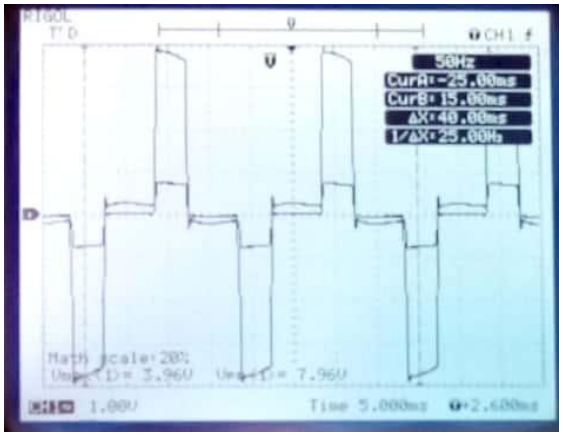


Fig 3.4.4: 3 level inverter waveform (Measured by CRO).

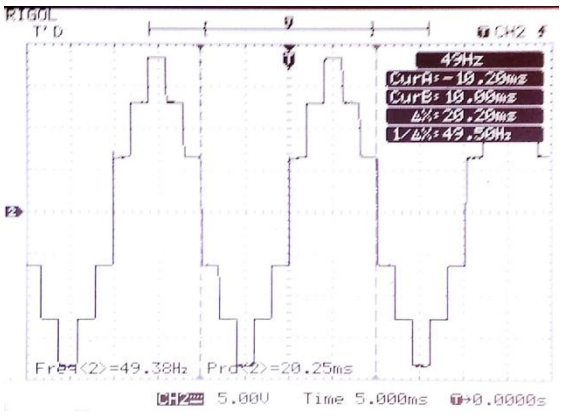


Fig 3.4.5: 7 level inverter waveform (Measured by CRO).

Analysis all experimental results following results are obtained as shown in table 2.

Table 2: Result

Sr.no.	Inverter	Current THD	Voltage THD
1	3 level	44.6%	62.9%
2	7 level	23.1%	20%

VI. CONCLUSION

By using the single phase cascaded H-bridge techniques for multilevel inverter is studied. Analyses of different level are compared. From analysis it is found THD content is 40 % less in 7 level than 3 level inverter. As levels are go on increasing harmonic content decreases but up to particular point only.

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