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8 Bit Processor with Customizable Architecture

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***Abstract*—Since its “birth” in 1971, embedded microprocessor has been widely used as a tool for technological innovations and cost reduction. Its speed and programmability are the main characteristics determining its performance.The demand for 8-bit processors nowadays is still going strong despite efforts by manufacturers in producing higher end microcontroller solutions to the mass market. Low-end processor offers a simple, low-cost and fast solution especially on I/O applications development in embedded system. In this paper we enroot to design an 8 bit microprocessor with customizable architecture.The project is the development of an 8 bit processor with the ability to customize its architecture. The project aims to build an 8 bit processor so that a user can try different architecture by arranging or connecting the building blocks in his/her own custom designs of a processor.**

***Keywords*—Logic IC – 8 Bit Processor, Arithmetic and Logic Unit (ALU)**

I. INTRODUCTION

The project is the development of an 8 bit processor with the ability to customize its architecture. The project aims to build an 8 bit processor so that a user can try different architecture by arranging or connecting the building blocks in his/her own custom designs of a processor.

This work is almost similar to the Arduino project or scratch project. Because the Arduino project was an open source project which helped, people with basic electronics knowledge, to write codes for a microcontroller in simple C program. And scratch was a visual programming language to help with coding. This allowed people to write their own programs very fast, without spending a lot of time for studying the programming language itself. Further details about Arduino and scratch can be found in their websites.

The project is about building 8 bit processor building blocks. Because if an entry level electronics student or people with basic electronics knowledge wish to design and test their own custom designs of a processor, the only cost effective way available is to try with a simulation software. But trying on a simulation software is very different from playing with hardware. Better simulation software are also a little costly.

II. BUILDING BLOCKS

A. Block Diagram

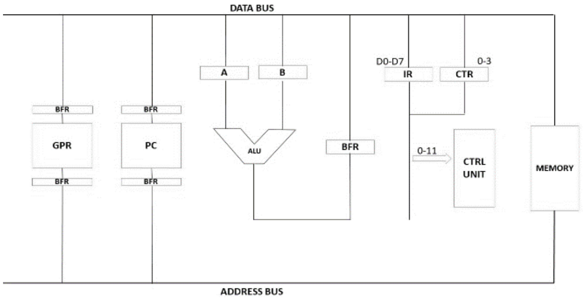

Fig. 1 Block Diagram of Proposed System

B. Building Blocks

*1) Arithmetic Logic Unit (ALU):*An arithmetic logic unit (ALU) is a combinational digital electronic circuit that performs arithmetic and bitwise operations on integer binary numbers. An ALU is a fundamental building block of many types of computing circuits, including the central processing unit (CPU) of computers, FPUs, and graphics processing units (GPUs). A single CPU, FPU or GPU may contain multiple ALUs.

ALU used for the project is 74181 The 74181 is a bit slice arithmetic logic unit (ALU), implemented as a 7400 series TTL integrated circuit.The 74181 represents an evolutionary step between the CPUs of the 1960s, which were constructed using discrete logic gates, and today's single-chip CPUs or microprocessors. Although no longer used in commercial products. It is also sometimes used in 'hands-on' college courses, to train future computer architects.

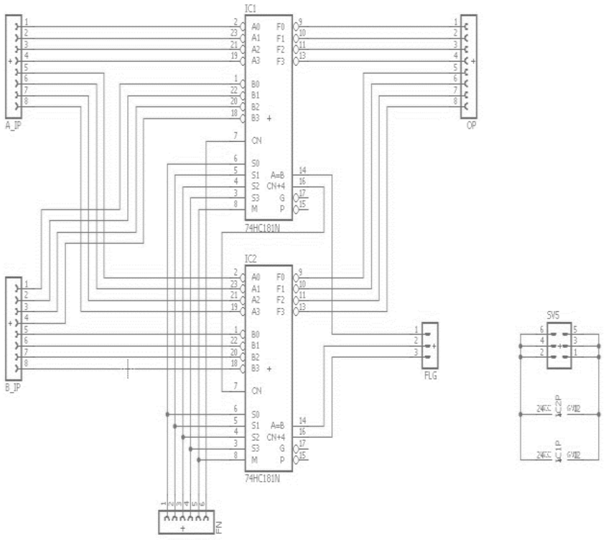

Fig. 2 ALU Circuit Diagram

*2) ALU Output Buffer:*ALU output buffer used for this project is 74574 which is octal D-type flip-flop with positive edge triggered. Data buffer (or just buffer) is a region of a physical memory storage used to temporarily store data while it is being moved from one place to another. Typically, the data is stored in a buffer as it is retrieved from an input device (such as a microphone) or just before it is sent to an output device (such as speakers). However, a buffer may be used when moving data between processes within a computer. This is comparable to buffers in telecommunication. Buffers can be implemented in a fixed memory location in hardware or by using a virtual data buffer in software, pointing at a location in the physical memory. In all cases, the data stored in a data buffer are stored on a physical storage medium. A majority of buffers are implemented in software, which typically use the faster RAM to store temporary data, due to the much faster access time compared with hard disk drives. Buffers are typically used when there is a difference between the rate at which data is received and the rate at which it can be processed, or in the case that these rates are variable, for example in a printer spooler or in online video streaming.

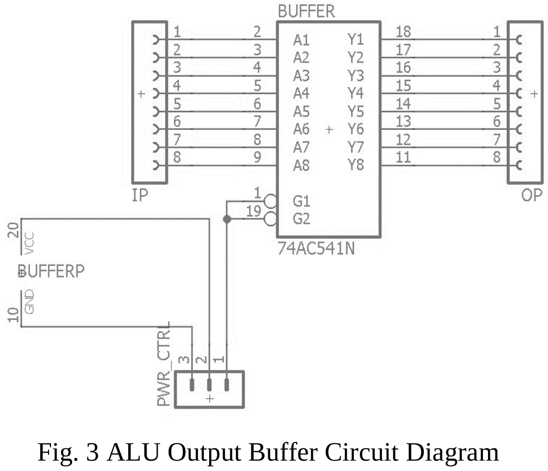

Fig. 3 ALU Output Buffer Circuit Diagram

3) A & B Registers:

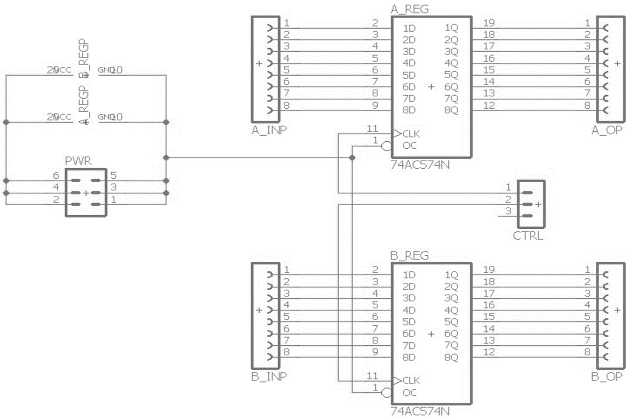

Fig. 4 A & B Registers

4) Control Unit: The control unit (CU) directs the operation of the processor. It tells the computer's memory, arithmetic/logic unit and input and output devices how to respond to a program's instructions. Control unit AT28C256 is used in this project which has many Functions. The Control Unit (CU) is digital circuitry contained within the processor that coordinates the sequence of data movements into, out of, and between a processor's many sub-units. The result of these routed data movements through various digital circuits (sub-units) within the processor produces the manipulated data expected by a software instruction (loaded earlier, likely from memory). It controls (conducts) data flow inside the processor and additionally provides several external control signals to the rest of the computer to further direct data and instructions to/from processor external destinations.

5) IR Circuit Diagram

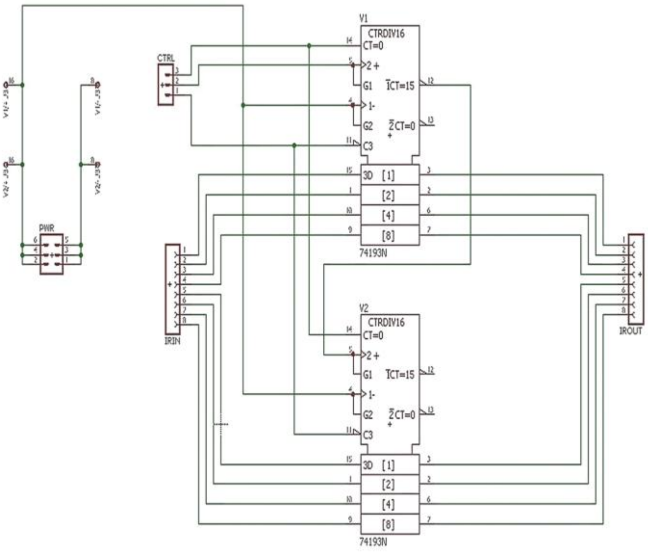

Fig. 5 IR Circuit Diagram

6) Instruction Counter: IC used for the designing of instruction cycle counter is 74193. Which execute the instructions in the instruction register .The DM74LS193 circuit is a synchronous up/down 4bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters. The outputs of the four master-slave flip-flops are triggered by a LOW-to-HIGH level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held HIGH. The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is LOW. The output will change independently of the count pulses.

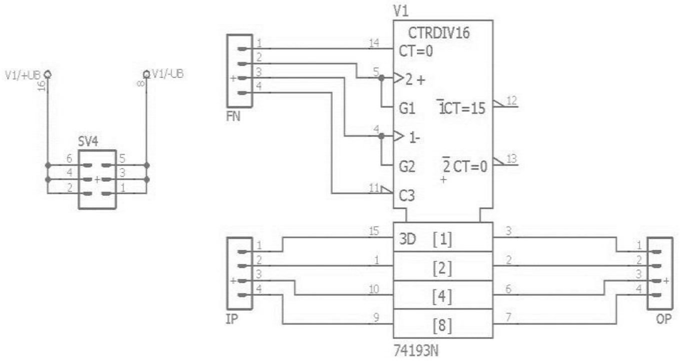

Fig 6 Instruction Counter Circuit Diagram

7) Program Counter: Program counter used in this project is 74Is193. A program counter is aregisterin a computerprocessorthat contains the address (location) of theinstructionbeing executed at the current time. As each instruction getsfetched, the program counter increases its stored value by 1. After each instruction is fetched, the program counter points to the next instruction in the sequence. When the computer restarts or is reset, the program counter normally reverts to 0.

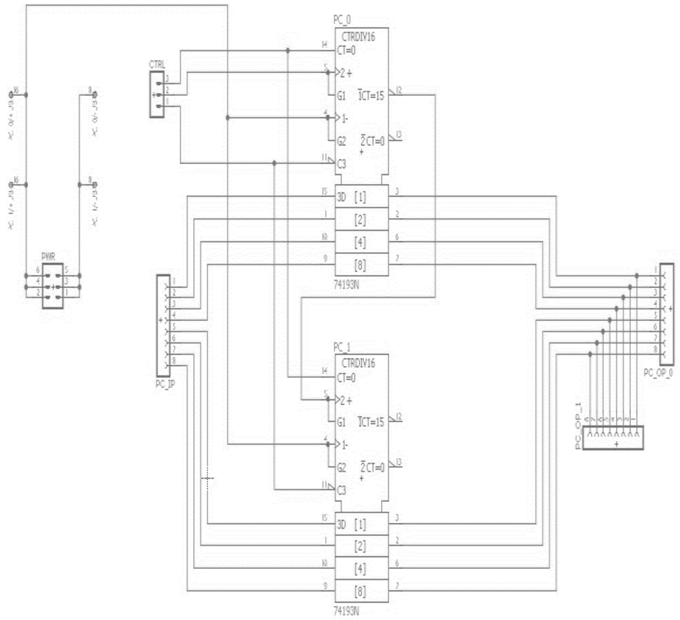

Fig. 7 Program Counter Circuit Diagram

8) General Purpose Register: The 74189 is a high-speed 64-bit RAM organized as a 16- word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-STATE and are in the high impedance state whenever the Chip Select (CS) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

9) Memory (AT28C64B): AT28C64B is the memory IC used in the processor. It is an 8 bit parallel EEPROM with a capacity of 8K. This memory IC is used as the program memory of the processor. And five of this IC is also used for producing the control signals. So with the five memory IC each with 8 bit data can provide 40 bit wide control signals, in other words the control signal bus width is 40 bits wide. The five memory IC used as micro programmed control unit is preprogramed with control signals for each instructions. This is done by dividing the 8K memory into 512 instruction blocks with each instruction block having a maximum capacity of 16 bytes. This means the 8K memory can store 512 different instructions and each instruction can have a maximum of 16 instruction cycles. The instruction block is selected by the opcode stored in the instruction register i.e., the opcode in the instruction register will act as the address for selecting the instruction block in the control unit. Combining the instruction cycle counter with the instruction register, the instruction cycle counter will act as the offset address for selecting different instruction cycles.

III. WORKING

The processor is made up of different sub blocks mainly ALU, General purpose register, Program counter, Instruction register, Control unit and Memory. All the sub blocks are 8 bit wide.

For the processor to work, the program is saved on an 8 bit memory IC. In the program each instruction is 8 bit wide and the operand is also 8 bit wide. Initially the processor starts from a reset when power on. The reset signal resets the program counter, instruction register, instruction counter and the interrupts. Instruction register is 8 bit wide with the functionality of incrementing and resetting the stored value. The instruction counter is a 4 bit up counter which counts at each clock edge. Combining the instruction counter and the instruction register 12 address lines are coming to the control unit memory. The least significant bits of the control unit address are from the instruction counter and remaining 8 bit address are from instruction register. So the control unit memory can be divided into 256 memory blocks each block with a size of 16 bytes.

1) Control Unit Working: In the control unit memory each block represents an instruction. The instruction cycle like fetch next instruction, increment program counter, A REG in etc. are programmed in the block. For example to load A register the instruction cycle will be:

- PC out, MMRY RD, IR in.
- INC PC.
- PC out, MMRY RD, A in.
- INC PC.
- RST CTR.

The above cycles are stored in a block. The particular block will be only used for loading A register. Similarly there will be another block for loading B register. Since instruction counter is 4 bit there can be a maximum of 16 cycles.

So each instruction will be represented by a block and the instruction cycle will be represented by bytes inside the block.

The instruction register selects the instruction block and the instruction counter selects each instruction cycle in the instruction block.

2) General Purpose Register: GPR is the general purpose register. In the processor two TTL RAM ICs are used as the general purpose register. Each IC is 4 bit wide so combining two results in an 8 bit general purpose register. Each IC have 16, 4 bit memory so there are 16 general purpose register. The input to the GPR is directly connected to the data bus. And the output are connected to both data bus and address bus through buffer. Each buffer can be activated to output the data to data bus or address bus. This is useful because when the data from GPR need to be send to memory or A register, it can be done by enabling GPR to DATABUS buffer. And when data in GPR is an address it can be directly send to ADDRESSBUS by enabling GPR to ADDRESSBUS. This is saves instruction execution time when addressing data from GPR.

3) Program Counter: PC is the program counter. The program counter is used to address each instruction in the memory. It is an 8 bit unit so the maximum memory size will be 256 bytes. The pc can be incremented and can be loaded. The pc can be loaded directly from the data bus and the output of the pc is connected to both data bus and address bus. The connection to data bus is useful when the address of next instruction need to be saved in a register. This is useful when using call instructions and interrupts.

4) ALU A Register and B Register: The ALU is designed using an ALU IC. The IC have all the required functions except divide and multiply. The input to the ALU is from the two registers A & B. The output is connected to both data bus and address bus through buffer. The output is also connected to flag logic unit where the flags are calculated.

*5) Instruction Execution:*Initially the processor starts from a reset. When reset the PC IR and IR counter will be reset to zero. So IR points to first instruction block. IR counter selects the first cycle in first block. So the first cycle which is PC out, MMRY RD, IR in will be executed. This loads the first instruction into the IR .when the instruction is loaded, at the same instant the instruction block will be changed to that particular instruction. At the second clock the second cycle from the selected block will be executed which is INC PC. This two cycles will be same for all the instruction blocks. The remaining cycles are different for different blocks. The fetched instruction will be executed by each cycle thereafter and when the instruction cycle ends it will be reset to initial position of the instruction block. The initial position which is the [PC out, MMRY RD, IR in] will be executed again from the instruction and at the instant of execution of this cycle the IR will be loaded with next instruction and at the same instant the instruction block will be changed to the new instruction block. Similarly the new instruction will be executed and this process continues.

IV. ADVANTAGES AND DISADVANTAGES

A. Advantages

- Working is visible.
- Can learn working of basic building blocks.
- Can test different instruction sets.
- Can design new instructions.

B. Disadvantages

- Large size.
- Low speed.
- Low memory capacity.
- High power consumption.
- Needs extra circuits.

V. CONCLUSION

The project aimed at the design and build of an 8 bit processor which can be fully customized in the CPU architecture level. It is mainly targeted for electronics hobbyists and electronics students. It helps anybody with a basic electronics knowledge irrespective of age to design and test a CPU. This also helps them to know a deep understanding of how a CPU is working in the register level and also helps to improve the concepts of digital electronics and programming.

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