International Journal of Technical Innovation in Modern Engineering & Science (IJTIMES)
Impact Factor: 3.45 (SJIF-2015), e-ISSN: 2455-2585
Volume 4, Issue 01, January-2018

ARCHITECTURE EFFICIENCY IN DUAL ZONE MODE DOUBLE PRECISION FLOATING POINT SECTION

[1]G Ramesh Reddy, [2]T Kalyani

[1]*Associate Professor, Electronics and Communication Engineering*
St.Martin's Engineering College, Dulapally, Secunderabad, T.S, India

[2]*Assistant Professor, Electronics and Communication Engineering*
MLR Institute of Technology, Dundigal, Hyderabad, T.S, India

ABSTRACT: Floating factor department is a centre range crunching extensively utilized as a part of logical and building packages. This paper proposed engineering for twofold precision floating point department. This engineering is meant for double mode usefulness, that can either check in on a couple of twofold precision operands or on two units of single precision operands in parallel. The engineering depends on the arrangement improvement multiplicative method of mantissa calculation. For this, a singular dual mode Radix-four Modified Booth multiplier is planned, which is applied iteratively in the design of double mode mantissa calculation. Other key components of floating factor division circulation, (as an instance, using one-identity, left/right specific shifters, adjusting, and so on.) are moreover re-intended for the double mode operation. The proposed double mode engineering is orchestrated utilising UMC 90nm innovation ASIC execution. Two sorts of proposed layout are exhibited, one with single stage multiplier and any other with two section multiplier. Contrasted with an independent twofold precision division layout, the proposed double mode engineering requires 17% to 19% additional gadget belongings, with 3% to five% length overhead. In comparison with in advance craftsmanship in this, the proposed design out-plays them concerning required vicinity, generation and throughput.

KEYWORDS: Radix-4, Required area, Power, Floating, Multiplier, Craftmanship.

1. INTRODUCTION:

Integer multipliers are the simple constructing blocks of many application regions, consisting of numerical processing, cryptography, and additionally as the main constructing block of floating factor multiplication [1]. Despite many advancement and lots of implementation strategies, the location necessities and performance numbers of this arithmetic operation is a bottleneck, especially when its length will increase. Floating factor range gadget is a common choice for plenty clinical computations because of its extensive dynamic variety characteristic. The unmarried precision and double precision floating factor arithmetic processing units are quite fashionable at the modern CPUs, GPUs and DSP processors. Increased precision necessities, leads to the switching from single precision to double precision in lots of application regions. A higher precision requirement than the double precision is wanted, thus we will see that using quadruple precision mathematics operation in many new packages.

2. PREVIOUS STUDY:

Very restrained work is available inside the literature for the quadruple precision arithmetic has stated the ASIC implementations of quadruple precision arithmetic. A recent work has suggested the implementation of quadruple precision multiplier on FPGA platform [2][3]. Obviously, our proposed work on green implementation of big integer multipliers and the quadruple precision floating point multiplication is very proper for FPGA as well as ASIC systems. In this painting, we've got proposed designs for large integer's multipliers, and its generalization for even larger integer multipliers. Further, the paper has prolonged their use for the mantissa multiplication of quadruple precision floating factor numbers. The layout has used "Karatsuba Multiplication" method, a famous multiplication principle, together with green use of FPGA assets [4]. Implementation of the multipliers leads to effective use of DSP48 blocks at the FPGA alongside different common-sense resources and promising overall performance. We have used Xilinx ISE synthesis tool, Model Sim SE simulation tool, and Xilinx Virtex-4 FPGA platforms for implementations and for result comparisons. The third approach for department is

iterative algorithms. One paintings the usage of iterative algorithms to put into effect a floating-point divider in FPGAs changed into presented by using Ressler and Nelson. Based on the Newton-Rapson set of rules and using repeated multiplication to approximate the end result, this algorithm calls for best multipliers. However, a small lookup desk may be brought to compute the end result of the primary little new release to lessen the whole range of iterations. Unlike the research desk based algorithms, larger floating-point layout

3. PROPOSED SYSTEM:

The proposed structure is proven in Fig. It is composed of three pipelined tiers. The subtle elements of every level engineering are pointed out underneath in following subsections one-by means of-one. Two sixty four- bit operands; one earnings (in1) and some other divisor (in2) are the crucial contributions along the mode manage flag dp_sp (twofold precision or double single precision). Both info operands either consists of DP operands (as whole sixty-four-bit combine) or parallel SP operands (as preparations of 32-bit fit), as seemed. The following two gadgets, the principle one indicator (LOD) and dynamic left shifter, on this degree perform sub-regular handling. They deliver the sub regular mantissa (assuming any) into the standardized arrangement. Initially it registers the degree of left move utilising double mode LOD and after that movements the mantissa with the double mode dynamic left shifter. The relating left moving sum is moreover balanced inside the kind. The layout for double mode LOD is seemed [5][6]. The double mode LOD is composed in a various levelled meld, making use of a critical constructing rectangular of two:1 LOD which contains of an AND, an OR, and a NOT gates. The closing 64:6 LOD unit contains of two 32:5 LOD units, which work one by one for SPs (on every 32-bit elements of records mantissa), and their yield combination offers the left-transferring upload up to DP mantissa. The complete assets in double mode LOD unit are shared among DP and SPs handling, and it costs no overhead contrasted with simply DP LOD.

4. SIMULATION RESULTS:

The proposed structure is proven in Fig. It is composed of three pipelined tiers. The subtle elements of every level engineering are pointed out underneath in following subsections one-by means of-one. Two sixty-four- bit operands; one earnings (in1) and some other divisor (in2) are the crucial contributions along the mode manage flag dips (twofold precision or double single precision). Both info operands either consists of DP operands (as whole sixty-four-bit combine) or parallel SP operands (as preparations of 32-bit fit), as seemed. The following two gadgets, the principle one indicator (LOD) and dynamic left shifter, on this degree perform sub-regular handling. They deliver the sub regular mantissa (assuming any) into the standardized arrangement. Initially it registers the degree of left move utilising double mode LOD and after that movements the mantissa with the double mode dynamic left shifter. The relating left moving sum is moreover balanced inside the kind. The layout for double mode LOD is seemed [7]. The double mode LOD is composed in a various levelled meld, making use of a critical constructing rectangular of two:1 LOD which contains of an AND, an OR, and a NOT gates. The closing 64:6 LOD unit contains of two 32:5 LOD units, which work one by one for SPs (on every 32-bit elements of records mantissa), and their yield combination offers the left-transferring upload up to DP mantissa [8][9]. The complete assets in double mode LOD unit are shared among DP and SPs handling, and it costs no overhead contrasted with simply DP LOD.

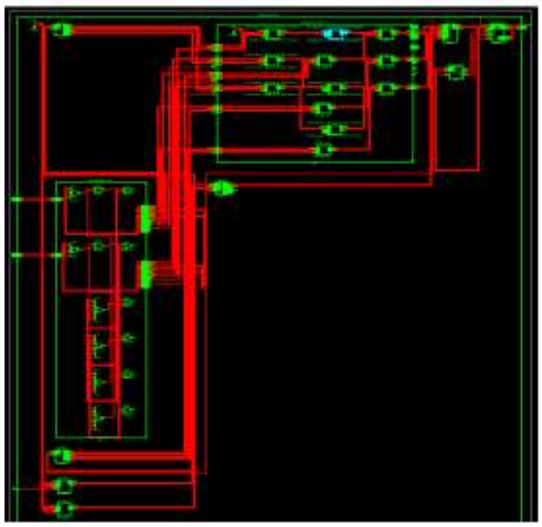

Fig.4.1. Developed circuit diagram.

5. CONCLUSION:

The proposed structure is established in Fig. It is composed of 3 pipelined levels. The diffused elements of each stage engineering are pointed out under in following subsections one-via-one. Two sixty 4- bit operands; one income (in1) and some other divisor (in2) are the important contributions along the mode manipulate flag dips (twofold precision or double unmarried precision). Both data operands either consists of DP operands (as entire sixty 4-bit integrate) or parallel SP operands (as preparations of 32-bit in shape), as seemed. The following gadgets, the principle one indicator (LOD) and dynamic left shifter, on this diploma perform sub-everyday dealing with. They supply the sub ordinary mantissa (assuming any) into the standardized association. Initially it registers the degree of left circulate using double mode LOD and after that moves the mantissa with the double mode dynamic left shifter. The touching on left transferring sum is moreover balanced within the type. The format for double mode LOD is seemed. The double mode LOD is composed in a numerous levelled meld, utilising a crucial building square of :1 LOD which includes of an AND, an OR, and a NOT gates. The last 64:6 LOD unit carries of two 32: five LOD units, which work one after the other for SPs (on every 32-bit factors of information mantissa), and their yield combination offers the left-shifting add up to DP mantissa. The complete belongings in double mode LOD unit are shared among DP and SPs handling, and it fees no overhead contrasted with without a doubt DP LOD.

REFERENCES:

[1]B. Lee and N. Burgess. Parameterizable floating-point operations on FPGA. In 36th Asilomar Conference on Signals, Systems and Computers, volume 2, pages 1064– 1068. IEEE Signal Processing Society, November 2002.

[2]G.Govindudu, R. Scrofano, and V. K. Prasanna. A library of parameterizable floating point cores for FPGAs and their application to scientific computing. In The 2005International Conference on Engineering of Reconfigurable Systems and Algorithms(ERSA 2005), June 2005.

[3]P. C. Diniz and G. Govindu. Design of FieldProgrammable Dual-precision Floating-Point Arithmetic Units. In Proceedings of the 16th international conference on field-programmable logic and applications (FPL'06), pages 733–736, August 2006.

[4]N. Shirazi, A. Walters, and P. Athanas. Quantitative analysis of floating point arithmetic on FPGA based custom computing machines. In IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), pages 155–162, April 1995. [5]J. Dido, N. Geraudie, et al. A flexible floating-point format for optimizing data-paths and operators in FPGA based DSPs. In ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA), pages 50– 55, February 2002.

[6]E.Roesler and B. E. Nelson. Novel optimizations for hardware floating-point units in a modern FPGA architecture. In 12th International Conference on FieldProgrammable Logic and Applications (FPL'02), pages 637–646, Sept. 2002.

[7]P.Surapong, F. A. Samman, and M. Glesner. Design and Analysis of Extension-Rotation CORDIC Algorithms based on Non-Redundant Method. In International Journal of Signal Processing, Image Processing and Pattern Recognition, vol. 5, no. 1, pp. 65–84, March 2012.

[8]K.Maharatna, S. Banerjee, E. Grass, M. Krstic, and A. Troya. Modified Virtually Scaling-Free Adaptive CORDIC Rotator Algorithm and Architecture. In IEEE Trans. on Circuits and Systems for Video Technology, vol. 15, no. 11, pp. 1463–1474, Nov. 2005.

[9]H. Hahn, D. Timmermann, B. Hosticka, and B. Rix. A Unified and Division-Free CORDIC Argument Reduction Method with Unlimited Convergence Domain Including Inverse Hyperbolic Functions. InIEEE Trans. on computers, vol. 43, no. 11, pp. 1339– 1344, Nov.1994.