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PROBABILISTIC BLUNDERS MODELING FOR APPROXIMATE ADDERS

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ABSTRACT: Approximate adders are used in applications that are error tolerant to save on power and area. Basically, in error resilient applications, approximate adders are used to obtain high performance gain. In this paper we presented a analytical model for approximate adders (i.e.) Probability Mass Function (PMF). This PMF unit consists of sub adder units which are in uniform as well as non-uniform lengths. A closed form of expression is derived for the error probability to obtain high performance. By using arbitrary input distributions the analytical part is determined. By using the proposed error model, we can estimate the probability of error in circuits with multiple approximate adders. The proposed error model is most widely used in practical applications of image processing. Therefore the proposed designs achieve the best tradeoff between accuracy, delay and power.

KEY WORDS: Approximate computing, adders, probability of error, probability mass function (PMF), image smoothing, modeling, arithmetic, analysis.

I.INTRODUCTION

Approximate computing is used in applications which are error tolerant, especially those involving speech and video. The error tolerance is exploited in designing computational systems to save on resources such as power, area and delay. Several approximate adders have been proposed and studied in the literature, each representing a trade-off between accuracy and resources. One possibility is to segment the adder into two parts. The upper part of the sum containing its most significant bits (MSBs) is obtained using accurate adders. Approximate logic is used to compute the Lower part of the sum containing the remaining least significant bits (LSBs).

There are other approximate adders which do not split the output into approximate lower part and accurate upper part. Instead, the adder is divided into many sub adders, where each of these sub adders use accurate full adders while the incoming carry to the sub adder is predicted and approximated. In these adders, we can trade off accuracy for a lower frequency of operation resulting in savings in power. However, these adders perform worse than the two-part segmented adders in terms of power-accuracy trade-off. The typical system optimization problem is to choose an added that meets the accuracy constraint with the lowest power. Doing Monte Carlo (MC) simulations within each iteration of the optimization is not practical. Analytical expressions for various error metrics will significantly speed up the process. Probabilistic error modeling has been done for those selected category of approximate adders which use sub adders and carry prediction between sub adders. Approximate circuits are also modeled and analyzed using a combination of Boolean analysis techniques and MC simulations.
A large number of such applications involve media processing, such as image, video and audio based applications designed for human interface. Other such computationally intensive applications include data mining and machine learning. A common feature in these applications is that they do not require the outcome to be fully precise, rather an approximate result is adequately acceptable. Approximate computing is an emerging trend in hardware and software design that exploits this inherent tolerance for inaccuracy for efficiency gain in terms of required hardware, speed and/or power. In order to select an appropriate approximate adder for a given application, comparative performance of the available designs has to be taken into consideration. The designs mentioned above have been evaluated and compared in terms of critical path delay, required hardware and power resources and error statistics. Traditionally, the error performance evaluation and comparison presented for these adders relies on computer simulations, which can only be executed exhaustively for small-sized adders. As the adders size grows, time and memory resources required for the exhaustive simulations render them infeasible or impossible. For deployment in any application, systematic quantification of the computational inaccuracy in these designs is indispensable. Unlike the existing statistical performance metrics that rely on Monte Carlo simulations, the proposed analytical model for probability of error provides an accurate measure for accuracy comparison of a wide variety of approximate adders.
In order to have a scalable and accurate error performance evaluation of approximate adders without the need of simulations, in this paper, we propose a generic methodology for analytical modeling of probability of error and Probability Mass

Function (PMF) of error value in the output of approximate adders. In the proposed methodology, the conditions on input that lead to error in the output are identified. These conditions are then systematically transformed into simpler, independent events and the probabilities of these events are analyzed in a general form for arbitrary input distributions. The probabilistic analysis is carried out using basic theorems of probability theory. The class of adders selected for the analysis include high-speed, low-latency approximate adders. These adders involve carry chain truncation and carry prediction between successive precise sub-adder units. A general model for this class of adders is presented for analysis that can be configured to any of the adders presented and the probability of error in their approximate sums can be computed using the proposed methodology.

The accuracy achieved using the proposed approach has been validated by ensuring that the probability of error and PMF of error are in concordance with simulation results. The main advantages of the proposed approach are: It facilitates comparison among arbitrary bit width approximate adders without the need of time-consuming simulations, which are always required to evaluate performance metrics used in existing works. Using the models developed by the proposed methodology, the error statistics can be expressed as functions of circuit parameters, like number of input bits, carry-chain length, number of overlapping prediction bits and number of sub-adders. Hence they can provide insights into the relationship between circuit specifications and error statistics, which can help the circuit designers choose circuit parameters according to application requirements. Since in most practical applications, circuits with multiple adders are used to perform more complex arithmetic operations, we also present an analysis for cascade of adders. Once the probability of error in an approximate adder in computed using the above-discussed methodology, it is used to compute error probability in circuits using multiple, independent approximate adders. The results are validated through Monte-Carlo simulations and for image processing applications.

The relaxation of the accuracy requirement for these applications potentially enlarges the design space, which may contain some solutions with smaller area, delay, and power consumption than those targeted for accurate computation. This leads to a new design paradigm, known as approximate computing, which deliberately sacrifices a small amount of accuracy to achieve improvement in performance and power consumption. In this work, we focus on designing approximate adder. As adders are key building blocks in many applications that are suitable for approximate computing, many previous works propose various designs of approximate adder These adders have smaller areas, delays, and power consumption compared to the accurate ones. Many of them also have small error rates. However, most of them cannot guarantee a small relative error in their outputs. As a result, they may degrade the output quality for some applications. Furthermore, these approximate adders are subject to sign calculation error when doing signed addition for 2's complement numbers.

II.RELATED WORK

The emerging paradigm of approximate computing has been applied at various levels of modern computing systems. For example, at the algorithm level, random sampling-based approaches can be viewed as approximate algorithms that trade off accuracy for the improvement in runtime. They have significant runtime advantage over the deterministic counterparts for many compute-demanding applications, such as high-dimensional integral and large matrix factorization. At the compiler level, loop perforation was proposed to skip a number of loops to accelerate the program at the cost of introducing some amount of error. At the architecture level, Esmaeilzadeh et al. proposed to execute compute-intensive approximable code on a neural network-based accelerator. Imani et al. proposed a resistive configurable associative memory that enables approximate matching induced by voltage over scaling.

At the circuit level, many approximate arithmetic circuits, such as adders, multipliers, and dividers, were proposed. For some applications, it is desirable to reconfigure the approximate circuits to achieve different accuracy requirements at runtime. For this purpose, several works also proposed additional error detection and correction modules. Also, techniques for analyzing specific approximate circuits were developed. For example, Masher et al. proposed a probabilistic error modeling method for a specific class of approximate adders that comprise of sub-adder unit. They also proposed a method for analyzing the error of approximate multipliers constructed from approximate partial product modules. Furthermore, several other works designed approximate circuits for specific error-tolerant applications, such as video encoding and artificial neural network. For a detailed survey of approximate computing, the readers can refer to the papers. Since adder is a basic module in many error-tolerant applications, researchers have proposed a number of approximate adders in the previous works.

One type of approximate adder uses an accurate adder to calculate the sum bits at the most significant positions, while applying a simple but inaccurate digital circuit to the remaining bits. For example, the Low-part-OR Adder (LOA) uses a simple OR gate to obtain the sum at lower bit positions and Error-Tolerant Adder I (ETAI) uses a modified XOR gate for the same purpose. This kind of design has a high error rate. Also, if the bit length of the accurate part is long, the delay and power consumption of the adder are still very large. Furthermore, its relative error will be large when doing addition on small input values. The author proposed a k-bit look ahead approximate adder to limit the carry chain for each bit in order to reduce the critical path. However, the area of this adder is large due to the fact that the computation of each bit needs an individual carry generator. The entire adder is divided into a number of blocks. The sum of each block is computed based on a speculated carry-in signal, which is obtained from the bits before the current block. This method effectively reduces the

critical path delay. However, it could introduce large relative error for the computation results, which may decrease the output quality for some applications. Furthermore, all of the approximate adders are subject to sign calculation error when doing signed addition for 2's complement numbers. Although after introducing an error reduction module, the relative error of CSAA can be reduced, it still fails to solve the problem on sign calculation. In contrast, the adder proposed in this work guarantees a small relative error. Furthermore, with the extra lightweight sign error correction module, it can always ensure the correct sign calculation.

A type of adder related to approximate adder is variable-latency adder, such as Variable Latency Carry Selection Adder (VLCSA) and the adder proposed. However, it is still an accurate adder. It consists of an underlying approximate adder and an error correction module. When the output of the approximate adder is correct, the computation is finished within one clock cycle. However, when an error occurs, a second clock cycle is needed to fix the error. Its performance highly depends on the applications. For situations where the probability of an error is large, a variable-latency adder has a higher chance to need the second clock cycle, which increases the total delay significantly.
Basically, error analysis is performed for arithmetic circuits with voltage over-scaling. The approach used is specific for arithmetic architectures for voltage over-scaled signal processing applications. a systematic methodology for Modeling and Analysis of Circuits for Approximate Computing (MACACO) has been proposed. Monte-Carlo simulations are used to compute metrics including error probability and error distribution. The methodology can be used to compare specific configurations of any approximate circuit but the error statistics and distributions obtained are numeric data that cannot be parameterized in terms of circuit specifications. Consequently, they cannot yield insights into its behavior dependencies and causalities. The probability of error in the ACA-II adder has been approximated. However, in this model, circuit's components and intermediary outputs have been assumed to be independent in order to simplify the analysis. The model does provide some understanding of error dependence on adder configuration but the computed frequency of error is only an approximation, which may deviate significantly from its exact value as the effects of interdependencies in the adder components become more pronounced. Additionally, it cannot be used to find the PMF of error.

III.PROPOSED PROBABILISTIC ERROR MODEL ANALYSIS

The N-bit approximate adder, is constructed using L sub-adders. The ith sub-adder, for i ¼ 1; 2; ... ; L, is a Ri þ Si-bit precise adder. The output of Sub-adder 1 is always correct as there is no loss of accuracy due to carry chain truncation. However, the outputs of Sub-adder 2 to Sub-adder L can be erroneous since addition with the carry generated by the previous less significant bits has been eliminated. Since the output sum is obtained by gathering the outputs of all the sub-adders, error in any sub-adder's output can contribute to error in the final output. Error in the ith sub-adder (for i 2) occurs when the Ri prediction bits of the sub-adder's input are all propagating carry-in and the previous less significant bits of adder's input, that are not input to this sub-adder, are generating carry-out.

The error occurs because the generated carry-out is not propagated due to the broken carry chain between sub-adders. Let E2; E3; ... ; EL represent events associated with the occurrence of error in Sub-adders 2; 3; ... ; L respectively. The error events are defined such that Ei ¼ 1 if the ith sub-adder output is erroneous and Ei ¼ 0 otherwise. Since any one of these events can contribute to error in the final output Sappr, the event associated with an error in Sappr is expressed as the union of these events. Furthermore, since two or more of these events can occur simultaneously, these events are not mutually exclusive. The probability of the union of such events can be evaluated using the inclusion-exclusion principle

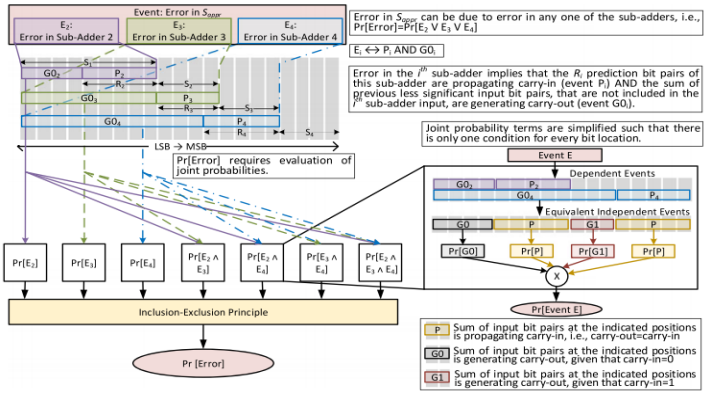


FIG. 1: PROPOSED PMF METHODOLOGY FOR THE PROBABILITY OF ERROR ANALYSIS.

The above figure (1) shows the architecture of probability error analysis for approximate adders. the entire system is determined under five steps they are given as, in the first step is to identify the errors in the intermediary logical elements of

the approximate adder that contribute to error in the output and then mathematically relate the occurrence of such errors with Pr½Error. In this step, Pr½Error will be expressed as the sum of probabilities of joint carry-in propagation and carry-out generation events for specified groups of input bits. The next step is to find each joint probability term. For this, we propose a method to transform these joint probabilities into products of probabilities of independent carry-in propagation and carry-out generation events. In third step, the probabilities of carry-in propagation and carryout generation events are derived in generalized form for arbitrary input distributions, which will be used to compute each product term. In fourth step, the analysis for the PMF of error value is presented. At last the proposed analysis is used to estimate the error statistics in circuits with multiple approximate adders.

For the ith sub-adder (i 2), the carry-in propagation event is defined for its Ri prediction bits and the carry-out generation event is defined for the previous less significant bits that are not included in the input of this sub-adder. Let G0i and Pi represent the carry-out generation (with carry-in equal to zero) and carry in propagation events that lead to error in the output of this ith sub-adder, respectively. Thus, the probability of intersection of independent events is equal to product of probabilities of individual events. It should be noted here that the input bits are perfectly independent if they are uniformly distributed and the probabilities of events Pi and G0i can be parameterized in terms of number of bits being added. In case of non-uniformly distributed inputs, these probabilities depend on both the number and position of bits and the events G0i and Pi may not be independent.

We found that the overlap in the events of carry-in propagation and carry-out generation is such that these events can be redefined or transformed into such equivalent events that are mutually independent. The equivalent events can be either carry-in propagation (P), carry-out generation with no carry-in (G0) or carry-out generation with carry-in equal to one (G1). In the proposed methodology, we have formulated a method for the transformation of dependent or overlapping events such that every input bit contributes to only one event. The three propagation events can be replaced by one propagation event, such that the new event imposes the propagation condition on all the bits involved in individual events. Now consider G02 and G03. Since there is a carry at the 5th bit position (due to G02) and next bits are propagating, then there will be a carry-out at the 7th bit position, which means that G03 is implied by G02 ^ P. Now, G04 implies a third carry at 12th bit position. However, P ^ G02 implies that there is a carry-out at the 10th bit location, which will also contribute to the sum at this bit location. Hence, G04 can be redefined as an event G1, i.e., a carry-out generation event at the 12th bit location with a carry-in at 10th bit location.

Now, we find the PMF of error value, aiming at understanding the distribution of this overall probability among all the possible error values. This is done by individually considering all possible error cases. In every case, error value is found by identifying the sub-adders with erroneous outputs and the weights of carry bits that are discarded due to the carry chain truncation. It was observed via simulations that if the approximate adders are cascaded, then the individual bits in the output of adders still remain approximately uniformly distributed. This is because sum from every single full adder can be 1 or 0 with equal probability. They are not exactly uniformly distributed because of the occurrence of error. However, since the occurrence of error is infrequent in most adder configurations, we found that the distribution of output bits is going to be very close to the uniform distribution. Thus the probability of error models remains approximately the same for every approximate adder and they can be applied by considering each adder as an independent component. We transform the dependent events into independent events according to the proposed methodology, as shown in Fig. 2.

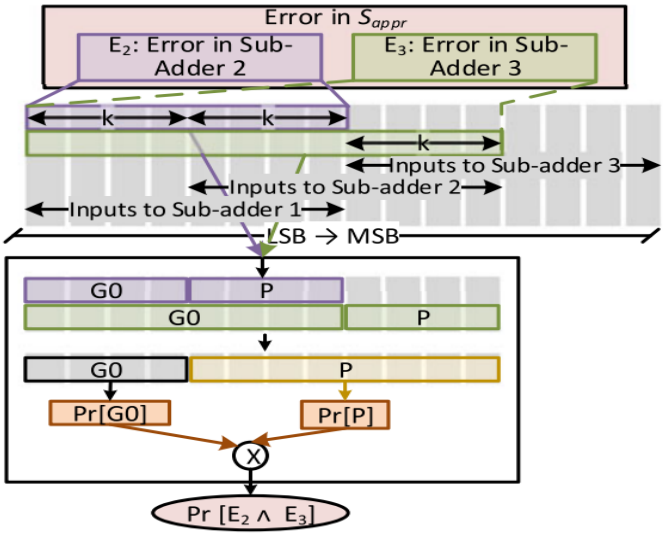
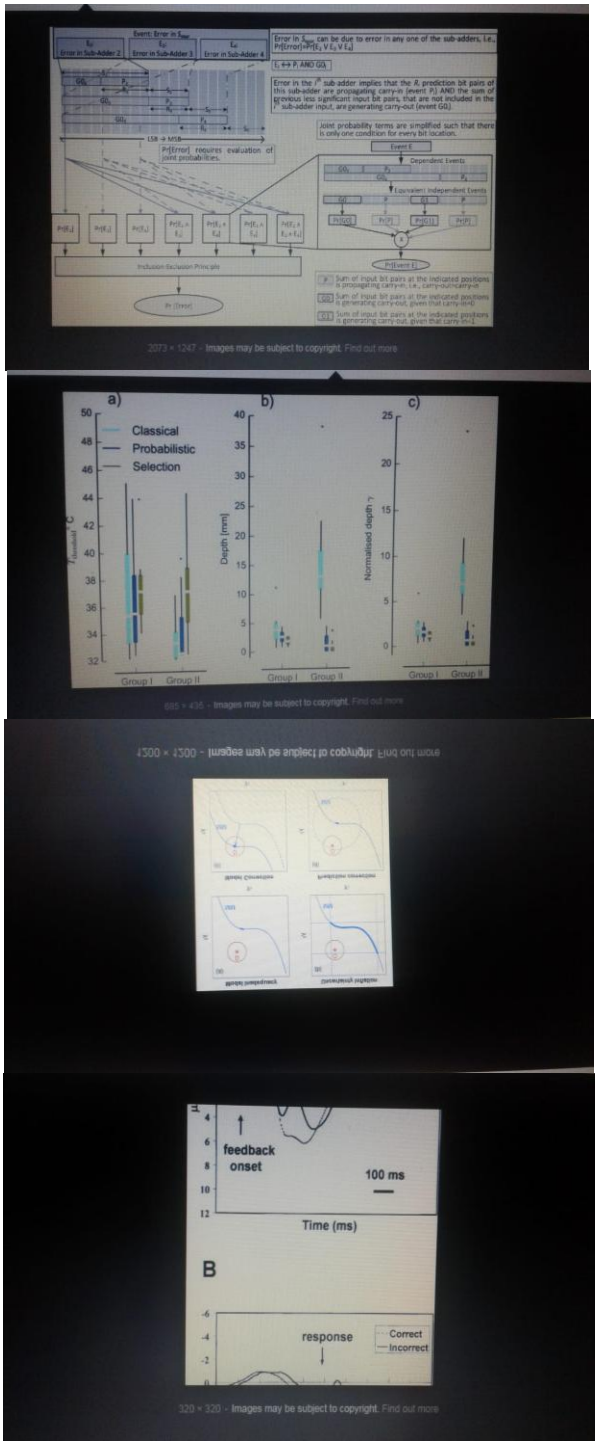


FIG. 2: DERIVATION OF PMF WITH FOUR SUB-ADDERS

This model assumes that the sub-adder outputs are independent of one another. The assumption simplifies the analysis but the model can compute only approximate probability of error. We found that the difference between exact probability of error and that predicted by the model increases as number of sub adders increases from three to five. Also with increasing number of input bits N, we found that this difference decreases and the exact probability of error approaches the approximation. This is because of the fact that with increasing N, if the number of sub-adders is kept constant, then the number of prediction bits increases in each sub-adder that in turn increases the probability of correct carry prediction and the outputs of different sub-adders become less inter-dependent. The accuracy enhances the reliability prediction of approximate adders and parameterization helps understanding the dependence of accuracy on various adder parameters, like size of adder and carry-chain length. These insights can be useful to the circuit's designers in building more predictable and reliable circuits.

IV. RESULTS



V.CONCLUSION

We have proposed a generic methodology to analyze the probabilistic error analysis for PMF model. For any given input distribution, the error statistics can be computed accurately without time-consuming exhaustive simulations. In applications using real data, the derived expressions are useful in predicting the performance of approximate adder. The methodology can be applied to calculate exact probability of occurrence of error and the PMF of error in any configuration of the adder model presented for given input distributions. The proposed methodology can serve as a useful tool for predicting comparative error performance of various configurations. This is illustrated in an image processing application, where PSNR is predicted accurately.

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