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A Literature Review on Various SRAM Architectures

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Abstract— Most of the devices that are used today are portable and it is highly necessary for these devices to have long battery life. The battery life of these gadgets is dependent on the power consumption of the components in the devices. The memory components are responsible for a major share of the power consumption and thus the memory components need to consume minimum power for efficient working of the device. We compare and examine the different SRAM cell architectures, 6T, 7T, 8T and 9T. The circuit and working of these SRAM cells are analysed and the advantages and disadvantages of each of the cells are discussed.

Keywords— SRAM, DRAM, WL, BL, BLB

I. INTRODUCTION

The current generation is highly dependent on the fast-evolving technology. The gadgets such as mobile phones, iPods, tablets and others are used by everyone on a daily basis. And so, these portable devices are expected to have a long battery life. The longer the operational time of these devices is, the more desirable they are to use. Thus, it is highly necessary that the components of the device consume less amount of power.
RAM devices are highly used as they allow the data that has been stored to be used or interfaced with, directly in any random method. There are mainly two kinds of RAM circuits, namely SRAM and DRAM.
DRAM is able to store a single bit of memory. This bit is stored in a capacitor but the circuit need not be refreshed for the bit to retain itself. But the circuit for SRAM is larger than the simple DRAM circuit and it is nevertheless volatile as during the time in which the power is not supplied to the circuit, the data will be lost.
In this paper, we analyze the various SRAM architectures, 6T, 7T, 8T and 9T. The circuit and the working of these SRAM cells are analyzed. The cells are also compared with each other to understand the differences in them and to know which architecture is more efficient in which ways.

II. EXISTING SRAM ARCHITECTURES

A. 6T SRAM ARCHITECTURE

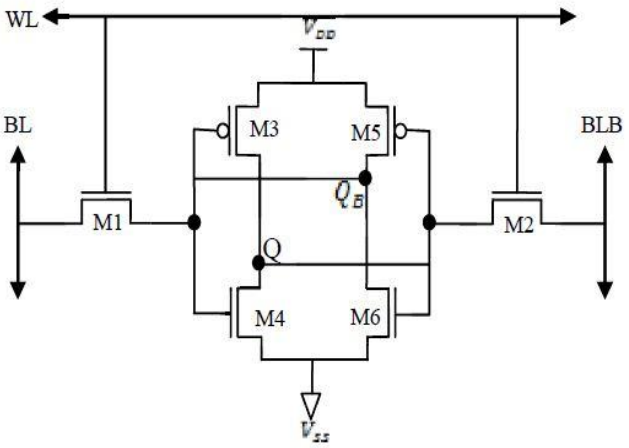

Fig. 1: The schematic diagram of the conventional 6T SRAM Cell.

A 6T SRAM unit is a kind of memory which stores information of one bit. Each bit is stored using a bistable latching circuitry. The main difference when compared with the dynamic RAM is that it does not require periodical restoring. Static RAM shows data remenance property, but if the memory is not supplied with power the data will be lost.
The 6T Static RAM consists about four transistors that form two inverters which are cross-coupled and two auxiliary transistors as access or pass transistors and that manages the storage unit access at the time of write cycle or read cycle operation. The 6T SRAM cell operations are the following:

a. STANDBY MODE

In STANDBY mode the circuit is said to be idle. A word_line (WL) is disabled in the standby mode, that is the word_line is equal to logical 0 then the access transistors M1 and M2 detaches the unit against the bit lines (Bit / Bitbar). During this time the two cross coupled inverters formed by the transistors M4 – M6continues to feedback mutually until the power supply is provided. The data will be held in the latch.

b. READ MODE

In READ mode, main task is to request the contents. The word_line (WL) should be made high to perform the read operation. That is, WL=1, the access transistors are enabled and connects the cell against the bit lines. To perform the read cycle operation, initially the memory should have some values. Therefore, consider that the cell has Q=1 the Bit and Bitbar acts as the output lines and the bit lines (Bit and Bitbar) are charged in advance to logical 1. The next step occurs when the data stored at the nodes are passed to the bit lines. Presume that logical 1 is saved at node so the Bitbar will discharge via the M4 and the Bit is pulled up byM3 to VDD, a logical 1.

c. WRITE MODE

In write mode, main task is to update the contents. Presume that logical 1 is already stored in the cell to write the information the data is applied on the bit line, Bit and the inverse data on the Bitbar, at that point the word_line is set to logical high to turn on the pass transistors. The inverter transistors are asserted by the driver of the bit lines as it is intense. When the content is saved in the inverters, the pass transistors can be made inactive and the inverter preserves the stored information.

B. 7T SRAM ARCHITECTURE

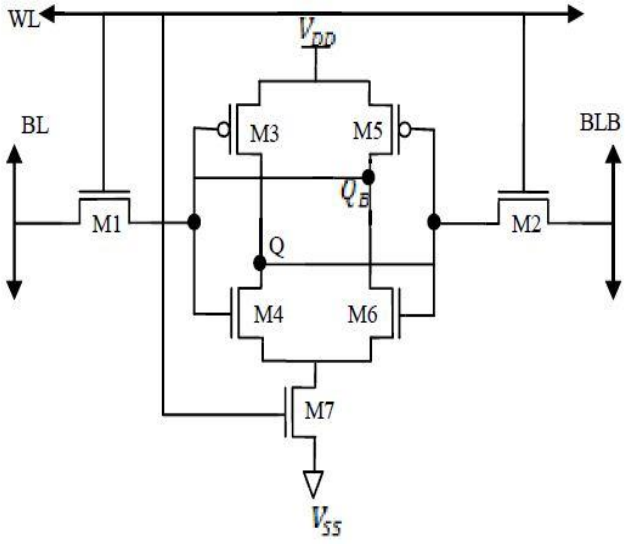

Fig. 2: The schematic diagram of a conventional 7T SRAM Cell.

The 7T SRAM architecture is cognate to the 6T SRAM architecture but there is an extra transistor in the 7T SRAM architecture. The extra NMOS transistor is enclosed by the cross-coupled inverters and the ground or vss. This extra transistor is denoted as M7 in Fig. 2. The gate terminal of the transistor is connected to the word_line; the drain terminal is associated to the cross-coupled inverter cell and the source node is connected to the ground.

The working is similar to the 6T SRAM architecture. The additional transistor acts as a gate power switch. It ensures that the power does not leak while the SRAM is in standby mode as the transistor M7 turns on only when the word_line, represented by WL in fig. 2, is high. The word_line is made high for the write and read operations while it stays low in stand-by mode. So, during the stand-by mode, the extra transistor M7 is inactive and ensures that the voltage does not pass through it to ground. Thus, the leakage power of the circuit is reduced when compared to 6T SRAM architecture. The 7T SRAM architecture thus gives a more efficient architecture while considering the power consumption but with a larger area.

C. 8T SRAM ARCHITECTURE

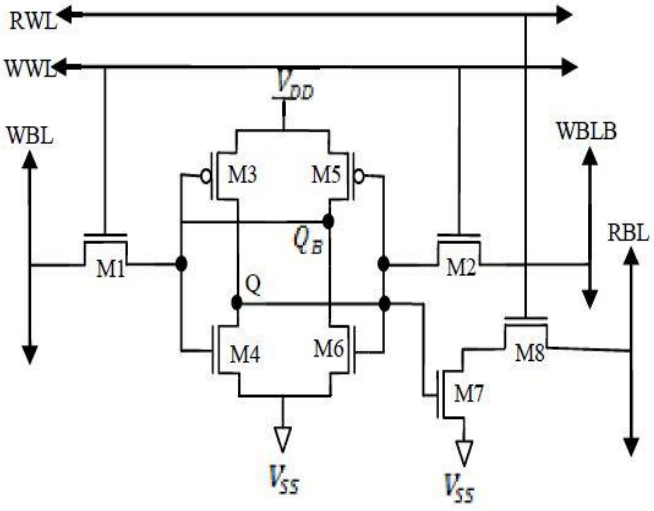

Fig. 3: The schematic diagram of the conventional 8T SRAM Cell.

The 8T SRAM cell architecture is comparable to the traditional 6T SRAM cell architecture but there are two additional transistors in the 8T SRAM cell architecture. The two additional transistors are denoted as M7 and M8 in the Fig. 3. The additional transistor M7 is used to decrease the gate leakage and the transistor M8 is used to free the cell static noise margin in the zero state. The static noise margin can be improved with the help of additional transistor M7, when cell holds logic '1'. The cell read noise margin of the 8T SRAM can be obtained by separating write and read operation.
The primary write and read operations of 8T SRAM are executed using single-ended sense amplifier. The 8T SRAM cell has less memory cell area when compared to the 9T SRAM cell due to the presence of single-ended amplifier. The write operation of 8T SRAM is same as the regular 6T SRAM cell. The 8T SRAM shows better variability tolerance as compared to the traditional 6T SRAM, due to which a secondary power supply is eliminated. The 8T SRAM cell is more adaptable than the traditional 6T SRAM cell due to better variability tolerance. Due to the presence of two additional transistors in the 8T SRAM, the cell area of 8T SRAM is increased as compared to the traditional 6T SRAM. The 8T SRAM cell has more successful way to increase the cell stability than a regular 6T cell..

D. 9T SRAM ARCHITECTURE

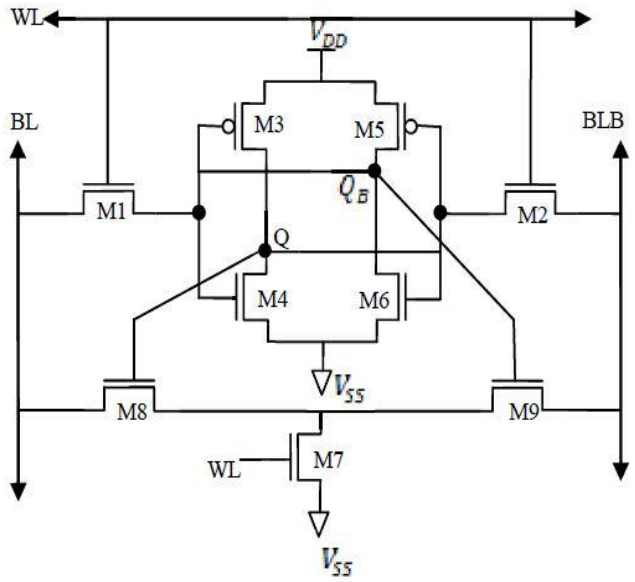

Fig. 4: The schematic diagram of the conventional 9T SRAM Cell.

It has 6T Static RAM architecture with 3 extra transistors. The three extra transistors are used for bypassing the read current from node referred as data storage. Upper sub circuit of 9T SRAM architecture forms the 6T SRAM cell. Transistors that are used to access bit lines and for read access forms lower sub circuit. Upper memory sub circuit is for

the application of storing data. Data stored within the Static RAM cell controls the functioning of the cell. Write signal is used for controlling the transistors used for write access.
To initiate write action WL = 1 and RD = 0. M1 and M2 are also equal to 1 during write operation. M8 and M9 can be changed for any changes in transistor M7. For the read operation WL=1 and RD=1. Transistor M7 is in saturation mode during read operation. Data will be isolated during read operation from bit lines. Also, for the time of read action 9T Static RAM cell is highly stable. Leakage power consumption can be reduced by setting the 9T Static RAM cell in a sleep mode called super cut-off. 9T SRAM architecture shows enhanced data stability and it consumes less power.

III. CONCLUSIONS

The variant topologies of Static RAM transistors have been reviewed. The 6T, 7T, 8T and 9T SRAM architectures have been studied and analysed. The operations of SRAM in different architectures are studied. The conventional 6T has the least count of transistors and are the most area efficient. The conventional 6T has the least count of transistors and it gives stability as well as it is the most area efficient. As the number of transistors increase, the area of the SRAM increases.

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