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An High Speed Ratioed CMOS circuit design with modified Pseudo Logic Circuits

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Abstract:

This paper evaluates the performance of ratioed logic circuit and conventional CMOS circuit at various CMOS technologies. As a part of this work 4 input NAND gate is designed using conventional CMOS and pseudo NMOS design with the help of DSCH2/ Microwind version 3.1 .The performance of both the circuits is compared interims of dissipated power and area .

I. Introduction:

The demand for speed ,reduced area and minimization of power consumption is increasing day by day in integrated circuits(ICs).The major setback of CMOS are increased area and power consumption. Weak pull up and strong pull down devices are used in ratioed circuits, which improves logical performance by eliminating large PMOS transistors loading the inputs based on the appropriate ratio of pull up to pull down strength. Ratioed circuits consume static power when the output is low. So they must be used where they are essential. A 4 input NAND gate is implemented using CMOS and pseudo NMOS logic gates on DSCH2 and Microwind. Number of transistors used to design pseudo NMOS is less than CMOS design .Different parameters such as power consumption, area ,rise delay, fall delay are compared for both the circuits at different CMOS technologies and simulation levels. Section II describes conventional CMOS design and section III explains pseudo NMOS design .Section IV describes the comparison of CMOS with pseudo NMOS design and result analysis. Section V concludes the paper.

II. Conventional CMOS design

The logic used in CMOS design effect the speed, area, delay and power consumption. The important characteristics of CMOS are high immunity to noise and low static power dissipation..One transistor of the pair is always kept in off mode, the other series connected transistor draws significant power during the switching operation between ON and OFF states. A schematic diagram of 4 input NAND gate with CMOS logic design is shown in the figure 1.8 MOS transistors are used to implement this design (4 pull up PMOS and 4 pull down NMOS).In the circuit when all the inputs are high ,all the NMOS transistors will conduct and a conductive path is developed between the output and ground (V_{SS}),which keeps the output low. If either of the output is high one of teh NMOS transistors will not conduct and one of the PMOS transistors will conduct. A conductive path will be developed between the output and V_{DD} which keeps output low.

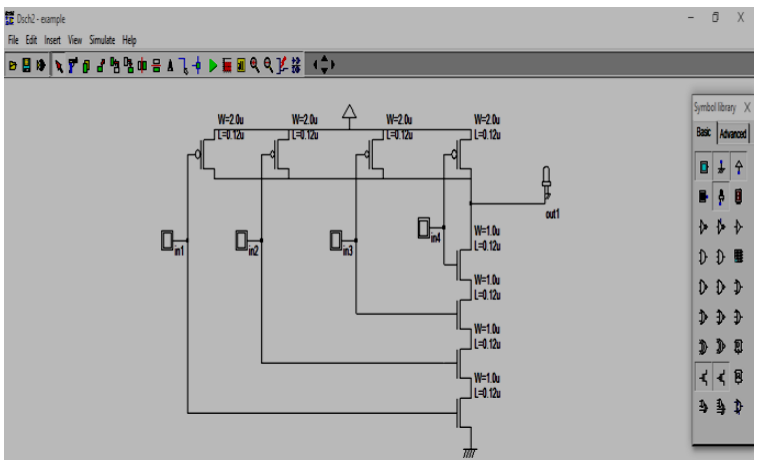

Figure 1: Schematic of4 input NAND gate using DSCH2

Figure1 can be implemented in Microwind using CMOS layout design tool .The layout ogthe design is implemented in the area of 19.9 μm^2

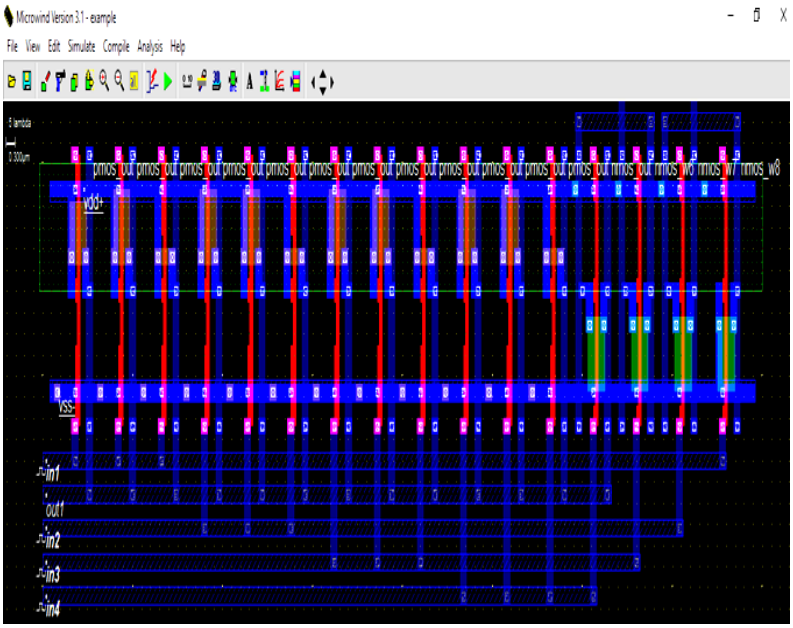

Figure 2: Layout of 4 input NAND gate using Microwind

III. Ratioed logic circuit

Weak pull up and strong pull down devices are used in ratioed circuits, which reduce the input capacitance and thus improve logical operation by eliminating large PMOS transistors loading the inputs. Schematic of 4 input NAND gate using pseudo NMOS logic gates is shown in the figure 3.The pull down network is like that of a static gate and pull up network is replaced by a single PMOS transistor and is grounded. Hence it is always in ON state . 4 input pseudo NMOS logic gate consist of 1 PMOS and 4 NMOS transistors. So number of transistors (6 transistors),area and complexity of the circuit is reduced. Since as less hardware is used in the circuit the capacitance is also reduced

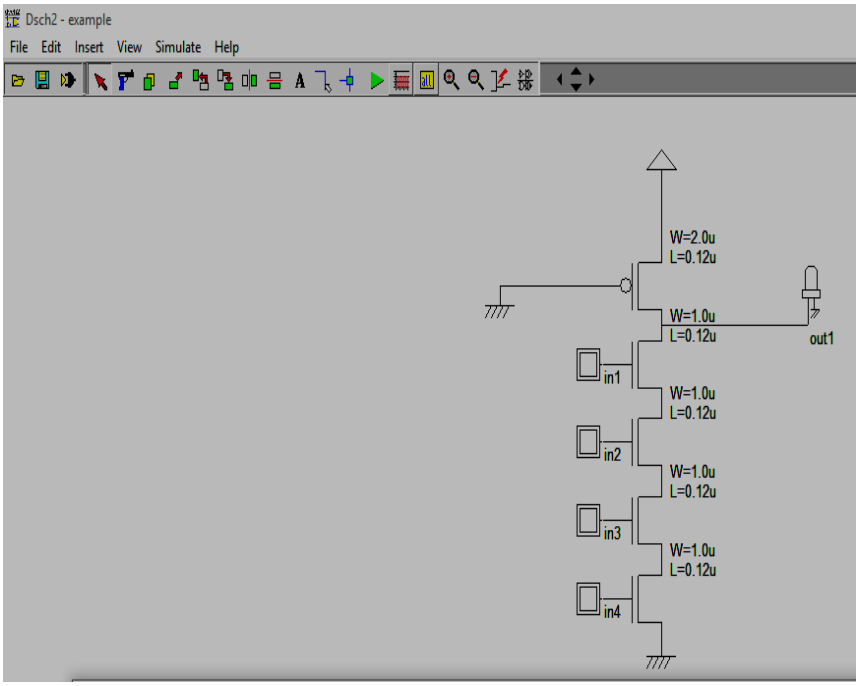

Figure 3:Schematic of 4 input NAND gate using ratioed logic using DSCH2

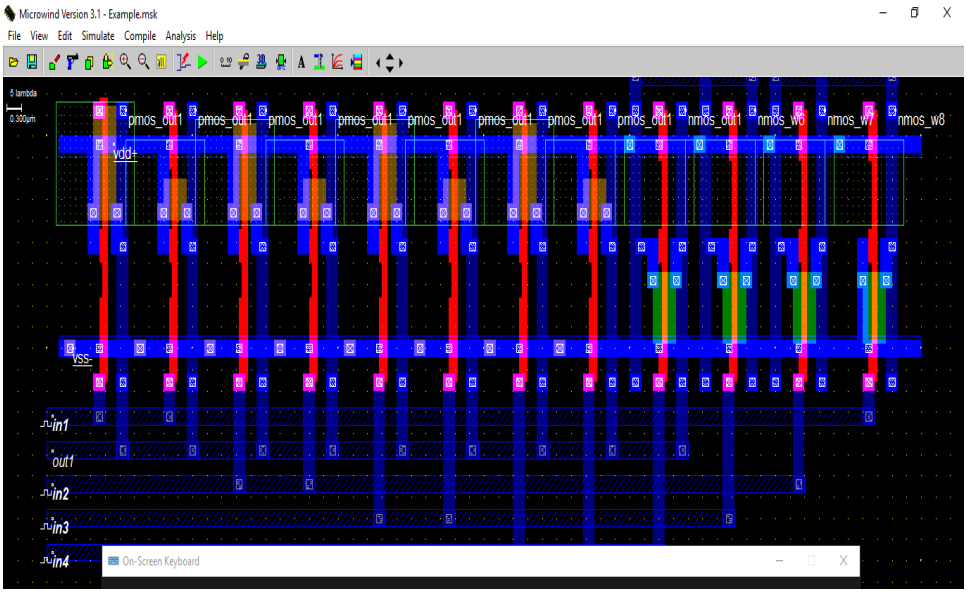

Figure 4:Layout of 4 input NAND gate using ratioed logic

IV. Comparison of result

Both 4 input NAND gate using CMOS and ratioed logic is implemented in Microwind for different CMOS technologies and at different simulation levels such as level-1,level-3 and BSIM-4.The parametric comparison is given in the ddtable-1.

CMOS Technology	**Width in µm**	**Length in µm**	**Area in µm^2**	**Simulation type**								
				Level-1			**Level-3**			**BSIM-4**		
				RD in PS	**FD in PS**	**PC µW**	**RD in PS**	**FD in PS**	**PC µW**	**RD in PS**	**FD in PS**	**PC µW**
0.12 µm	24.1	7.4	179.5	4*Ps*	0	2.416	4	16	1.899	3	21	1.642
0.18 µm	40.2	12.4	498.5	8*Ps*	37	17.622	9	52	10.894	9	74	9.915
0.25 µm	50.3	15.5	778.9	13	40	64.07	13	57	38.07	14	87	26.529
32nm	8	2.5	**19.9**	4	0	**0.044**	4	0	0.129	5	52	0.056
35nm	80.4	24.8	1993.9	42	120	0.322	44	188	0.154	44	204	0.130
45nm	10.1	3.1	31.2	4	0	0.082	4	15	0.182	9	42	0.080
65nm	14.1	4.3	61.1	0	0	0.466	0	0	0.573	0	25	0.379
90nm	20.1	6.2	124.6	0	0	1.67	0	0	1.578	0	20	1.56
SOI 0.12 µm	24.1	7.4	179.5	3	0	0.709	3	16	0.682	4	26	0.613

RD :Rise delay, FD: Fall delay ,PC: Power consumed

Table 1: Parametric analysis of 4 input NAND gate at different CMOS technologies and simulation levels

From table 1 and table-2 we analyze that a 4 input NAND gate requires an area of 19.9 µm^2 (8 µm×2.5 µm) with a rise delay of 4 *Ps* and consumes 0.044 µW of power when implemented in 8 metal 32nm CMOS technology. When ratioed logic is implemented at same technology requires 59.3 µm^2 (16.2 µm×3.7 µm), with no delay and consumes 2 *nW* of power .For the applications where area is of prime important the 4 input NAND gate using CMOS technology is preferred. But for some applications area is not a criteria and power consumption is very important in such cases ratioed logic can be chose .4 input NAND gate using CMOS requires very less area to implement and ratioed logic consumes very less power at the expense of area.

CMOS Technology	Width in µm	Length in µm	Area in µm^2	Simulation type								
				Level-1			Level-3			BSIM-4		
				RD in PS	FD in PS	PC µW	RD in PS	FD in PS	PS µW	RD in PS	FD in PS	PC µW
0.12 μm	48.6	11	533.6	0	0	0.075	0	0	0.075	0	0	0.075
0.18 μm	81	18.3	1482.3	0	0	0.433	0	0	0.432	0	0	0.432
0.25 μm	101.3	22.9	2396.1	0	0	1.039	0	0	1.035	0	0	1.035
32nm	16.2	3.7	**59.3**	0	0	**2nW**	0	0	2nW	0	0	2nW
35nm	162	36.6	5929.2	0	0	6.684	0	0	6.613	0	0	6.609
45nm	20.3	4.6	92.6	0	0	3nW	0	0	3nW	0	0	3nW
65nm	28.3	6.4	181.6	0	0	0.012	0	0	0.012	0	0	0.012
90nm	40.5	9.2	370.6	0	0	0.058	0	0	0.058	0	0	0.058
***SOI* 0.12 μm**	48.6	11	533.6	0	0	0.031	0	0	0.031	0	0	0.031

RD :Rise delay, FD: Fall delay ,PC: Power consu0med

Table 1: Parametric analysis of 4 input NAND gate at different CMOS technologies and simulation levels

Type	Technology used	Area in µm^2	Power
CMOS logic	32 nm	19.9	0.044 **µW**
Ratioed logic	32 nm	59.3	2 nW

Table 3: performance analysis of CMOS and ratioed logic at 32nm CMOS technology using level-1 design

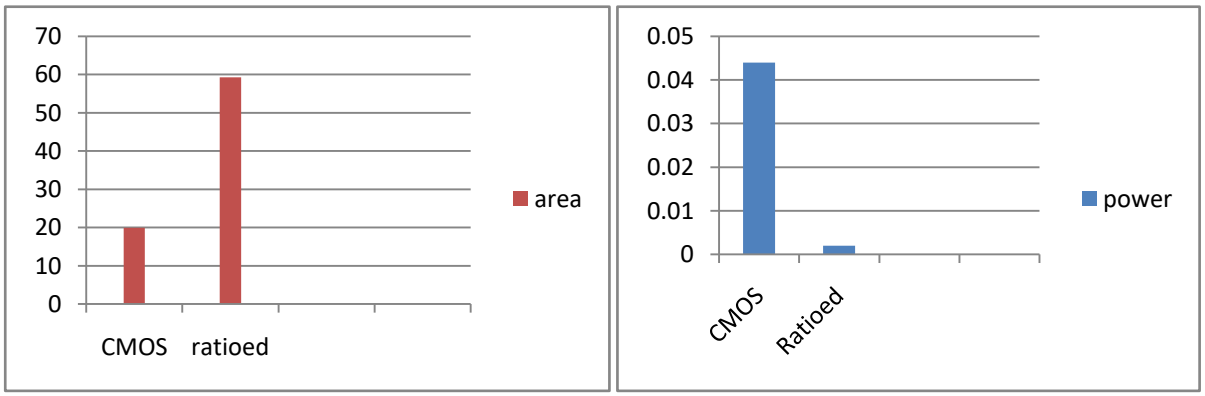

Figure 5: comparison of implemented area and dissipated power **in** CMOS and ratioed logic

V. Conclusion :

In this paper a 4 input NAND gate logic is compared with 4 input NAND gate using ratioed logic at diffe4rent CMOS technologies and simulation levels.4 input NAND gate with CMOS require less area and 4 input NAND gate with ratioed logic consumes less power. In the future , this work can be examined at different supply voltages, various forward and reverse biases and at various input capacitances.

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