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MODELING AND ANALYSIS OF A NEW NEGATIVE OUTPUT BUCK-BOOST CONVERTER WITH WIDE CONVERSION RATIO (DUTY CYCLE)

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Abstract— In this work, a new negative output (N/O) buck-boost converter, which can be applied for applications that need wide range of inverse voltage, is proposed. It is the modification of traditional buck-boost converter and provides inverse output voltage with wide conversion ratio. The steady state, small signal model and power losses of the proposed converter operating in continuous conduction mode (CCM) are analyze. Comparisons among the traditional buck-boost converter, N/O hybrid buck-boost converter and N/O self-lift Luo converter are presented, and it is found that the proposed converter possesses a widest voltage conversion ratio in these four converters. The configuration of the proposed new buck-boost converter circuit is simulates in MATLAB/ SIMULINK.

Keywords— DC-DC power converters, negative output, wide conversion ratio

I. INTRODUCTION

DC -DC converters have been applied to applications widely during the past few decades. With rapid development of technology, negative output (N/O) dc-dc converters play an important role in the industrial fields, such as regenerative braking system (RBS) of DC motors for hybrid electric vehicles, signal generator and data transmission interface, neutral point clamping power electronics systems, wind power generation and photovoltaic power generation[1]-[4], etc.

As well known, the buck-boost converter and Cuk converter are two typical traditional N/O converters, and their voltage conversion ratios ($-D/(1-D)$, that D is the duty cycle) are same. They can generate a higher or lower output voltage value than the input voltage. Theoretically, they both can produce an extremely high step-down or step-up output voltage when the duty cycle D is close to 0 or 1. However, in practical operation,this situation can not be met for the limitation of power switches and diodes [5], [6]. Additionally, a transformer can be used to get a larger conversion ratio, such as flyback converters which also obtain negative output voltage. Unfortunately, the transformer causes switch voltage overshoot and EMI problems that lead to low efficiency and huge volume [7].

In the past few decades, many N/O converters have been proposed. For example, the N/O KEY buck converter with the voltage conversion ratio $-D$ who had the fast load transient response was proposed in [8]. The N/O KY buck-boost converter with the voltage conversion ratio $-2D$ who possessed no bilinear characteristics was proposed in [9]. The N/O KY boost converter which was constructed by integrating a positive to negative path to boost converter with the voltage conversion ratio $-1/(1-D)$ was proposed in [10]. For wider conversion ratio, the voltage lift technique is applied to buck-boost or Cuk converter, such as the N/O self-lift Luo converter [1], the enhanced N/O self-lift Cuk converter [2], the N/O super-lift converter [11] and the voltage-lift-type Cuk converters [12]. However, all the above N/O converters have an unreasonable defect, that is, there is abruptly changing on the voltage across the energy-transferring capacitor which results in a very high current spike flowing through it. This capacitor's current spike which is only limited by the parasitic parameters [13] cause inherent power loss and EMI [14].

In [15], several N/O single-switch quadratic PWM converters were proposed. Although they have different structures, they share the same voltage conversion ratio $-D^2/(1-D)$. They can be regarded as modified cascading connection of buck and buck-boost converters, and require only one switch and three diodes. They have high step-down ability and wider conversion ratio than the traditional buck-boost converter. In [16] and [17], switched networks are inserted in the Cuk converter to construct the N/O hybrid Cuk converters. In [18], switched networks are inserted in the buck-boost converter to get hybrid buck-boost converters.

One N/O hybrid buck-boost converter with voltage conversion ratio being $-D/((1-D)(2-D))$ uses a switched-capacitor (SC) structure while another N/O hybrid buck-boost converter whose voltage conversion ratio is $-2D/(1-D)$ uses a switched-inductor (SL) structure. Nevertheless, the added switched networks lead to more diodes, capacitors or inductors to achieve wider conversion ratio, and it results in complex circuit, heavy volume and more power losses. In [19], a single-stage switched-capacitor-inductor N/O boost converter with the voltage conversion ratio $-1/(1-D)$ was proposed. However, an additional resonant inductor should be used to limit the current spike caused by the energy transfer capacitor. A new N/O buck-boost converter is proposed in this paper. It is a modification of the buck-boost converter and provides inverse output voltage with wide conversion ratio. This new converter uses the energy-transferring capacitor to store energy, and there is no abruptly changing voltage on it. The rest of the paper is organized as follows. The operating principle and steady state analysis of the proposed converter are described in Section II, and its small signal model is established in Section III.Power loss analysis is presented in section IV. MATLAB SIMULINK simulations are depicted in section V to verify theoretical analysis preliminary. A prototype is built and experimental results are presented for further validation in section V. Finally, some conclusions and remarks are presented in section VI.

II. STEADY-STATE ANALYSES

As presented in Fig. 1, the new negative output converter consists of an input voltage v_{in}, two power switches S_1 and S_2, two diodes D_1 and D_2, two inductors L_1 and L_2, two capacitors C and C_0, and one resistive load R. For steady-state theoretical analysis, it is assumed that all components are ideal and the proposed converter operates in CCM.

A.Operating Principle

Power switches are turned on and off simultaneously, so there are two operation stages that are shown in Fig. 2(a) (the first stage when the power switches are turned on) and Fig. 2(b) (the second stage when the power switches are turned off). Currents through L_1 and L_2 are denoted by i_{L1} and i_{L2},respectively.The voltage across the capacitor C is defined as v_C,and the voltage across the output capacitor C_0 is defined as v_0.

Some typical time domain wave forms are shown in fig 3,

Where N is nature number.

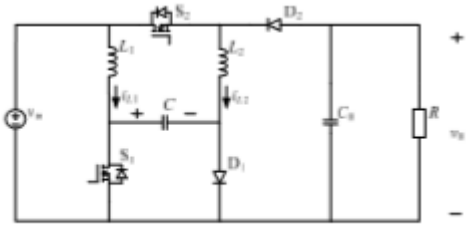
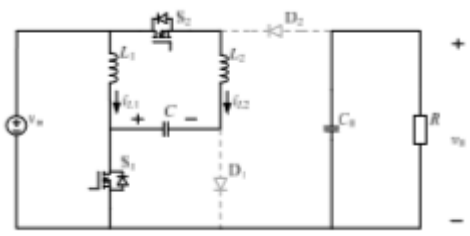


Fig. 1. New negative output buck-boost converter

1) First Stage

Power switches S_1 and S_2 are turned on during the subinterval (NT, $NT+DT$) in switching period as shown in Fig. 2(a), and diodes D_1 and D_2 are blocked via the reversal voltage. In this stage, the input voltage v_{in} supplies the energy to the inductor L_1, and the capacitor C together with the input voltage v_{in} delivers the energy to the inductor L_2. The voltage across the capacitor C is equal to the voltage stress on the diode D_1. The difference value of the input voltage v_{in} and the output voltage v_0 equals the voltage stress on the diode D_2.

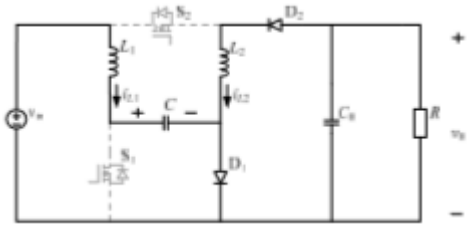


The corresponding differential equations can be given as follows

$$\left.\begin{aligned} L_1 \frac{di_{L1}}{dt} &= V_{in} \\ L_2 \frac{di_{L2}}{dt} &= V_{in} + V_c \\ C \frac{dv_c}{dt} &= -i_{L2} \\ C_0 \frac{dv_0}{dt} &= -\frac{V_0}{R} \end{aligned}\right\} \quad (1)$$

2) Second Stage

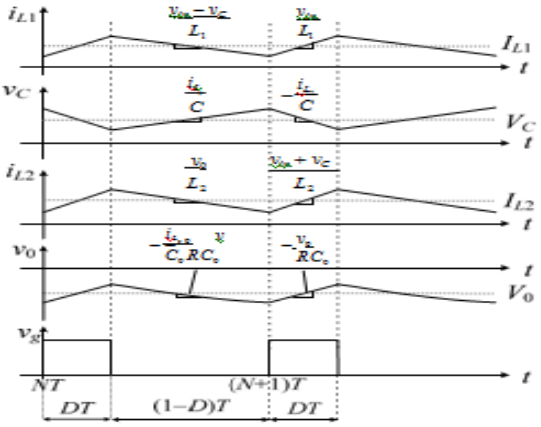
Power switches S1 and S 2 are turned off during the subinterval (NT+DT, NT+T) in any switching period as shown in Fig. 2(b), and diodes D1 and D2 conduct during this interval. Combining with the input voltage vin, the inductor L1 supplies energy to the capacitor C through the diode D1. Meanwhile, the inductor L2 transfers energy to the output capacitor C0 through the diodes D1 and D2. The voltage stress on the power switch S1 is equal to the voltage across the capacitor C, and the voltage stress on the power switch S2 equals vin–v0.



The associated differential equations can be derived as follows

$$\left.\begin{aligned} L_1 \frac{di_{L1}}{dt} &= V_{in} - V_c \\ L_2 \frac{di_{L2}}{dt} &= V_0 \\ C \frac{dv_c}{dt} &= i_{L1} \\ C_0 \frac{dv_0}{dt} &= -i_{L2} - \frac{V_0}{R} \end{aligned}\right\} \quad (2)$$

Fig. 3. Typical time-domain waveforms of the proposed converter.



B. Voltage Conversion Ratio

It is assumed that Vin, V_C, I_{L1}, IL2, I0 and V0 are corresponding DC values of vin, vC, iL1, iL2, i0 and v0. When the proposed converter is in steady state, inductors L1 and L2 satisfy the volt-second balance, that is, the net volt-seconds in one period is equal to zero.

$$\left.\begin{aligned} DV_{in} + (1\text{-}D)(V_{in}\text{-}V_C)=0 \\ D(V_{in}+V_C) + (1\text{-}D)V_0 =0 \end{aligned}\right\} \quad (3)$$

Accordingly, VC and V0 can be derived from (3) and the results are

$$V_C = \frac{1}{1-D}V_{in} \quad (4)$$

$$V_0 = -\frac{D(2-D)}{(1-D)^2}V_{in} \quad (5)$$

Consequently, the voltage conversion ratio of the proposed converter can be derived from (5) and its expression is

$$M=\frac{V_0}{V_{in}} = -\frac{D(2-D)}{(1-D)^2} \quad (6)$$

Obviously, if the duty cycle D is smaller than 0.29, the voltage conversion ratio M is less than 1, that is the proposed converter works in step-down mode. Otherwise, it works in step-up mode.

C. Voltage Stresses on Power Switches and Diodes

From the first stage, the voltage stresses on diodes can be obtained as follows

$$V_{D1} = \frac{1}{1-D}V_{in} \quad (7)$$

$$V_{D2} = \frac{1}{(1-D)^2}V_{in} \quad (8)$$

From the second stage, the voltage stresses on power switches are expressed as

$$V_{S1} = \frac{1}{1-D}V_{in} \quad (9)$$

$$V_{S2} = \frac{1}{(1-D)^2}V_{in} \quad (10)$$

D. Current Stresses on Power Switches and Diodes

Capacitors C and C0 satisfy the charge balance principle when the proposed converter is in steady state. We can obtain the expressions for IL1 and IL2 as follows

$$I_{L1} = \frac{D}{(1-D)^2} I_0 \quad (11)$$

$$I_{L2} = \frac{1}{1-D} I_0 \quad (12)$$

where the output current I0=V0/R. According to the operating principle, the current through the power switch S1 is

$$i_{S_1}(t) = \begin{cases} i_{L_1}(t) + i_{L_2}(t) & (NT, NT+DT) \\ 0 & (NT+DT, NT+T) \end{cases}. \quad (13)$$

Consequently, the dc value of iS1 can be calculated as

$$I_{S1} = \frac{D}{(1-D)^2} I_0 \quad (14)$$

By the same way, the dc value of the current through the power switch S2 is

$$I_{S2} = \frac{D}{1-D} I_0 \quad (15)$$

From the operation stages, the current through the diode D1 is

$$i_{D_1}(t) = \begin{cases} 0 & (NT, NT+DT) \\ i_{L_1}(t) + i_{L_2}(t) & (NT+DT, NT+T) \end{cases}. \quad (16)$$

Thus, the dc value of iD1 can be given by

$$I_{D1} = \frac{1}{1-D} I_0 \quad (17)$$

By using the same process, the dc value of the current through the diode D2 can be derived as

$$I_{D2} = I_0 \quad (18)$$

E. Variation Ratio of Current and Voltage

From the typical time-domain waveforms as shown in Fig. 3, one can see that the inductor current iL1 increases during the first subinterval and then decreases during the second subinterval. Thus, the peak-to-peak current ripple and the variation of the current iL1 can be calculated as follows.

$$\Delta i_{L_1} = \frac{V_{in} DT}{L_1} \quad (19)$$

$$\varsigma_1 = \frac{\Delta i_{L_1} / 2}{I_{L_1}} = \frac{(1-D)^2 TR}{2|M|L_1}. \quad (20)$$

Moreover, the peak-to-peak current ripple and the variation of iL2 are calculated as

$$\Delta i_{L_2} = \frac{D(2-D)V_{in}T}{(1-D)L_2} \quad (21)$$

$$\varsigma_2 = \frac{\Delta i_{L_2}/2}{I_{L_2}} = \frac{(1-D)^2 TR}{2L_2}. \quad (22)$$

Furthermore, the peak-to-peak voltage ripple and the variation of the voltages vC and v0 can be derived, and their expressions are

$$\Delta v_C = \frac{D^2(2-D)}{(1-D)^3}\frac{V_{in}T}{RC} \quad (23)$$

$$\varepsilon_C = \frac{\Delta v_C/2}{V_C} = \frac{D|M|T}{2RC} \quad (24)$$

$$\Delta v_0 = \frac{D^2(2-D)}{(1-D)^2}\frac{V_{in}T}{RC_0} \quad (25)$$

$$\varepsilon_0 = \frac{\Delta v_0/2}{V_0} = \frac{DT}{2RC_0}. \quad (26)$$

F. Boundary of CCM and DCM

The boundary between continuous and discontinuous conduction mode is that the minimum value of the inductor current equals zero, that is, 11 = /2 LL Ii □ and 22 = /2 LL Ii □ . Substituting (11), (12), (19) and (21) into these two equations, the condition for the proposed converter working in continuous conduction mode can be derived as follows

$$L_1 > \frac{(1-D)^4 TR}{2D(2-D)} \quad (27)$$

$$L_2 > \frac{(1-D)^2 TR}{2}. \quad (28)$$

G. Comparisons with Other Negative Output Converters

The traditional buck-boost converter, the N/O self-lift Luo converter and the N/O hybrid buck-boost converter utilizing the SL structure are compared with the proposed converter. Fig. 4 depicts their voltage conversion ratios. Note that, the vertical axis is the absolute value of their voltage conversion ratios. Also, the comparisons about the voltage conversion ratio, the voltage stresses on power switches and diodes, the number of components and the abruptly changing on the voltage among these converters have been presented in Table I. From Fig. 4, the maximum ideal step-up voltage conversion ratio of the proposed converter is around 24, which is much higher than other N/O converters at D=0.8, and its step-down

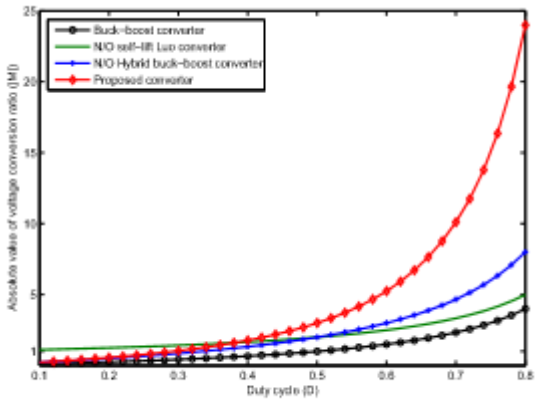


Fig. 4. Absolute value of the voltage conversion ratio against *D*.

Items	**Buck-Boost Converter**	**N/O Self-lift Luo Converter**		**N/O Hybrid Buck -Boost Converter**		**Proposed Converters**	
V_s	$\frac{1}{1-D}V_{in}$	$\frac{1}{1-D}V_{in}$		$\frac{1+D}{1-D}V_{in}$		S_1	$\frac{1}{1-D}V_{in}$
						S_2	$\frac{1}{(1-D)^2}V_{in}$
V_D	$\frac{1}{1-D}V_{in}$	D_1	$\frac{1}{1-D}V_{in}$	D_1	$\frac{2D}{1-D}V_{in}$	D_1	$\frac{1}{1-D}V_{in}$
				D_2	$\frac{D}{1-D}V_{in}$		
		D_2	$\frac{1}{1-D}V_{in}$	D_3	V_{in}	D_2	$\frac{1}{(1-D)^2}V_{in}$
				D_4	$\frac{1+D}{1-D}V_{in}$		
M_{CCM}	$-\frac{D}{1-D}$	$-\frac{1}{1-D}$		$-\frac{2D}{1-D}$		$-\frac{D(2-D)}{(1-D)^2}$	
Number of Switches	1	1		1		2	
Number of Diodes	1	2		4		2	
Number of Inductors	1	2		2		2	
Number of Capacitors	1	3		1		2	
Abruptly changing voltage	No	Yes		No		No	

voltage conversion ratio is comparable with the N/O hybrid buck-boost converter while the N/O self-lift Luo converter only provides a higher output voltage value. Hence, it is obvious that the proposed converter has a wider voltage conversion ratio. From Table I, clearly, there is no abruptly changing on the voltage across the energy-transferring capacitor C of the proposed converter, whereas the N/O self-lift Luo converter has abruptly changing voltage on the energy-transferring capacitor that causes extremely high current through the capacitor and switches. Compared with the N/O self-lift Luo converter and the hybrid buck-boost converter, the proposed converter has one more power switch. However, the N/O hybrid buck-boost converter needs four diodes and N/O self-lift needs three capacitors.

III. SMALL SIGNAL MODEL

As well known, small signal model is used to derive open loop transfer functions which are the basis of consequent control design and dynamical behavior analysis [19-22]. Here, the small signal model of the proposed converter is established, and the control-to-output transfer function is derived. Its bode diagrams calculated in the step-down and step-up mode are both presented and compared with the MATLAB SIMULINK simulated results. Based on averaging method, the state-average model can be directly derived as follows.

$$\begin{cases} L_1 \dfrac{d\langle i_{L_1}\rangle}{dt} = d\langle v_{in}\rangle + (1-d)(\langle v_{in}\rangle - \langle v_C\rangle) \\ L_2 \dfrac{d\langle i_{L_2}\rangle}{dt} = d(\langle v_{in}\rangle + \langle v_C\rangle) + (1-d)\langle v_0\rangle \\ C \dfrac{d\langle v_C\rangle}{dt} = -d\langle i_{L_2}\rangle + (1-d)\langle i_{L_1}\rangle \\ C_0 \dfrac{d\langle v_0\rangle}{dt} = -d\dfrac{\langle v_0\rangle}{R} + (1-d)(-\langle i_{L_2}\rangle - \dfrac{\langle v_0\rangle}{R}) \end{cases} \quad (29)$$

where $\langle v_{in}\rangle$, $\langle v_C\rangle$, $\langle i_{L_1}\rangle$, $\langle i_{L_2}\rangle$ and $\langle v_0\rangle$ are averaged values of v_{in}, v_C, i_{L1}, i_{L2} and v_0.

By superimposing small ac perturbation ˆin v and ˆ d which are far less in the magnitude compared to dc quiescent values, the averaged input voltage, the averaged duty cycle, the averaged currents through inductors L1 and L2, and the averaged voltages across capacitors C and C0 can be expressed as the sum of the dc values and the ac variations, that is

$$\begin{cases} \langle v_{in} \rangle = V_{in} + \hat{v}_{in} \\ \langle i_{L_1} \rangle = I_{L_1} + \hat{i}_{L_1} \\ \langle i_{L_2} \rangle = I_{L_2} + \hat{i}_{L_2} \\ \langle v_C \rangle = V_C + \hat{v}_C \\ \langle v_0 \rangle = V_0 + \hat{v}_0 \\ d = D + \hat{d} \end{cases} \text{ with } \begin{cases} |\hat{v}_{in}| \ll |V_{in}| \\ |\hat{i}_{L_1}| \ll |I_{L_1}| \\ |\hat{i}_{L_2}| \ll |I_{L_2}| \\ |\hat{v}_C| \ll |V_C| \\ |\hat{v}_0| \ll |V_0| \\ |\hat{d}| \ll |D| \end{cases} \quad (30)$$

Submitting (30) into (29), and neglecting the second and higher ac terms since their values are very small, we can derive the small signal model as follows

$$\begin{cases} L_1 \dfrac{d\hat{i}_{L_1}}{dt} = \hat{v}_{in} - (1-D)\hat{v}_C + \hat{d}V_C \\ L_2 \dfrac{d\hat{i}_{L_2}}{dt} = D(\hat{v}_{in} + \hat{v}_C) + \hat{d}(V_{in} + V_C) + (1-D)\hat{v}_0 - \hat{d}V_0 \\ C \dfrac{d\hat{v}_C}{dt} = -D\hat{i}_{L_2} - \hat{d}I_{L_2} + (1-D)\hat{i}_{L_1} - \hat{d}I_{L_1} \\ C_0 \dfrac{d\hat{v}_0}{dt} = -\dfrac{\hat{v}_0}{R} - (1-D)\hat{i}_{L_2} + \hat{d}I_{L_2} \end{cases} \quad (31)$$

By using Laplace transform on (31), the control-to-output transfer function Gvd(s) can be given by

$$G_{vd}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)} = \frac{V_{in}}{(-1+D)^3} \frac{b_3 s^3 + b_2 s^2 + b_1 s + b_0}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (32)$$

where

$$\begin{cases} a_0 = (-1+D)^4 R \\ a_1 = L_2(1-D)^2 + D^2 L_1 \\ a_2 = ((-1+D)^2 C L_1 + C_0(L_2 - 2DL_2 + D^2 L_1 + D^2 L_2))R \\ a_3 = C L_1 L_2 \\ a_4 = C C_0 L_1 L_2 R \end{cases} \quad (33)$$

$$\begin{cases} b_0 = 2(-1+D)^4 R \\ b_1 = -D(2-D)(D(L_1 - 2L_2) + L_2 + D^2(L_1 + L_2)) \\ b_2 = C L_1 R(-1+D)^2(2-D) \\ b_3 = C L_1 L_2 D(2-D) \end{cases} \quad (34)$$

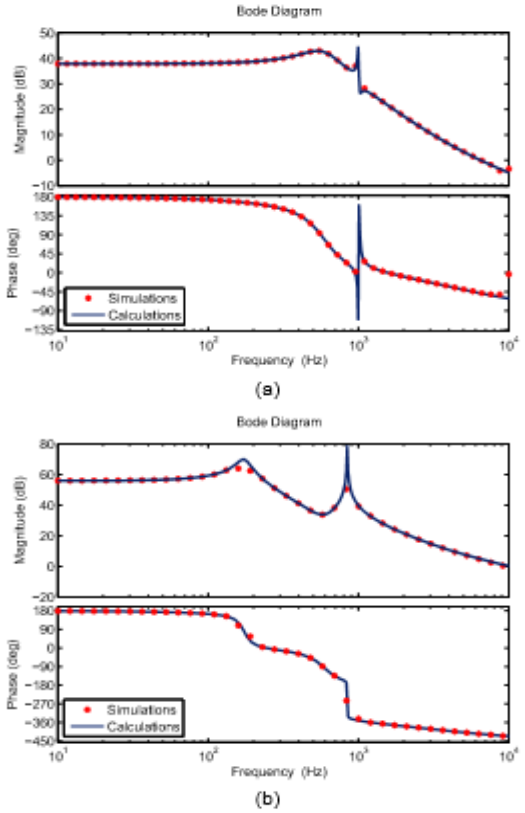


Fig. 5. Bode diagrams of $G_{vd}(s)$ from theoretical calculations and PSIM simulations (a) step-down mode; (b) step-up mode.

In order to confirm the derived control-to-output transfer function, comparisons of the bode diagrams from the theoretical calculations and the MATLAB SIMULINK simulations under Vin=20V, L1=0.8mH, L2=1mH, C=22μF and C0=44μF are shown in Fig. 5. Fig. 5(a) shows the case for step-down mode with the duty cycle D being 0.2 and the resistive load R being 10Ω. Fig. 5(b) shows the case for step-up mode with the duty cycle D being 0.6 and the resistive load R being 100Ω. It is clear that the theoretical calculations are in good agreement with the MATLAB SIMULINK simulations. Thus, the derived small signal model here is an effective model to describe the dynamical behaviors of the proposed converter.

IV. POWER LOSS ANALYSIS

The theoretical analysis above is based on ideal components without parasitic resistances. However, the design of converter must consider the power loss such as inductor copper loss, power loss associated with semiconductor forward drops and resistance [23]. Power loss of the proposed converter is analyzed in this part. Note that, here, the RMS represents the root-mean-square value.

A. Power Losses of Inductors

The power loss of inductor has copper loss caused by winding resistance rL and core loss caused by hysteresis and eddy current in the magnetic core. The copper loss places an important role in the total power loss of inductor [20]. According to (11) and (12), the approximate RMS values of currents through inductors are

$$I_{L_1(rms)} = \sqrt{\frac{\int_0^T i_{L_1}^2(t)dt}{T}} \approx \frac{DI_0}{(1-D)^2} \qquad (35)$$

$$I_{L_2(rms)} = \sqrt{\frac{\int_0^T i_{L_2}^2(t)dt}{T}} \approx \frac{I_0}{1-D}. \qquad (36)$$

The copper losses of inductors can be calculated from (35) and (36) as follow

$$P_{L\_C} = I_{L_1(rms)}^2 r_{L_1} + I_{L_2(rms)}^2 r_{L_2} = \left(\frac{D^2 r_{L_1}}{(1-D)^4 R} + \frac{r_{L_2}}{(1-D)^2 R} \right) P_0 \quad (37)$$

where the output power P0 equals to V0I0.

The core loss density of inductor can be approximated from the curve fit loss equation

$$\Delta P_{L\_Co} = aB^b f^c \quad (38)$$

where a, b and c are determined from curve fitting given

from the date sheet and the B is defined as half of the AC flux swing. Thus, the core losses of inductors are as follow

$$P_{L\_Co} = l_{e_1} A_{e_1} \Delta P_{L_1\_Co} + l_{e_2} A_{e_2} \Delta P_{L_2\_Co} \quad (39)$$

where le is the path length and Ae is the cross section of the core.

Hence, the total power losses of inductors are the sum of core loss and copper loss, that is

$$P_L = P_{L\_C} + P_{L\_Co}. \quad (40)$$

B. Power Losses of Capacitors

The power loss of capacitor is caused by parasitic resistance rC. Based on instantaneous currents in different operation stages, the approximate RMS values of currents through capacitors can be given by

$$I_{C(rms)} = \sqrt{\frac{\int_0^{DT} i_{L_2}^2 dt + \int_{DT}^{T} i_{L_1}^2 dt}{T}} \approx \frac{\sqrt{D}}{(1-D)^{3/2}} I_0 \quad (41)$$

$$I_{C_2(rms)} = \sqrt{\frac{\int_0^{DT} i_0^2 dt + \int_{DT}^{T} (i_0 + i_{L_2})^2 dt}{T}} \approx \sqrt{\frac{D}{1-D}} I_0. \quad (42)$$

Power losses of capacitors can be calculated by the following expression

$$P_C = I_{C(rms)}^2 r_C + I_{C_2(rms)}^2 r_{C_2} = \left(\frac{D r_C}{(1-D)^3 R} + \frac{D r_{C_2}}{(1-D) R} \right) P_0. \quad (43)$$

C. Power Losses of Power Switches

MOSFET is chosen as the power switch for the proposed converter. Its main power loss includes that the conduction loss caused by ON resistance rDS when it is turned on and the switching loss caused during the rise time tr and the fall time tf. The conduction loss of power switch depends on the ON resistance rDS and the RMS value of current through the power switch. Based on instantaneous currents in different operation stages, the approximate RMS values of currents through power switches are calculated as

$$I_{S_1(rms)} = \sqrt{\frac{\int_0^{DT} (i_{L_1} + i_{L_2})^2 dt}{T}} \approx \frac{\sqrt{D}}{(1-D)^2} I_0 \quad (44)$$

$$I_{S_2(rms)} = \sqrt{\frac{\int_0^{DT} i_{L_2}^2 dt}{T}} \approx \frac{\sqrt{D}}{1-D} I_0. \quad (45)$$

Hence, the conduction losses of power switches are

$$P_{S\_C} = I_{S_1(rms)}^2 r_{DS_1} + I_{S_2(rms)}^2 r_{DS_2} = \left(\frac{D r_{DS_1}}{(1-D)^4 R} + \frac{D r_{DS_2}}{(1-D)^2 R} \right) P_0 \quad (46)$$

The switching loss of power switch is related to the rise time tr, the fall time tf, the voltage stress across the power switch VS and the averaged current through it. Thus, the switching losses of power switches can be given by

$$P_{S\_S} = V_{S_1} I_{S_1} (t_{r_1} + t_{f_1}) f / 2 + V_{S_2} I_{S_2} (t_{r_2} + t_{f_2}) f / 2 = \left(f \frac{(t_{r_1} + t_{f_1}) + (t_{r_2} + t_{f_2})}{2(1-D)(2-D)} \right) P_0. \quad (47)$$

Accordingly, the total power losses of power switches are the sum of the conduction losses and the switching losses, that is

$$P_S = P_{S\_C} + P_{S\_S}. \quad (48)$$

D. Power Losses of Diodes

The power loss of diode is mainly caused by the forward voltage drop VF and the series resistance rD. Based on the instantaneous currents in different operation stages, the approximate RMS values of currents through diodes can be obtained as

$$I_{D_1(rms)} = \sqrt{\frac{\int_{DT}^{T} (i_{L_1} + i_{L_2})^2 dt}{T}} \approx \frac{1}{(1-D)^{3/2}} I_0 \quad (49)$$

E. Calculated Efficiency

The total power losses of the proposed converter is the sum of the power losses of inductors, capacitors, power switches and diodes, that is

$$P_{Loss} = P_L + P_C + P_S + P_D. \quad (52)$$

Thus, the calculated efficiency of the proposed converter can be given by

$$\eta = \frac{P_0}{P_0 + P_L + P_C + P_S + P_D}. \quad (53)$$

V. SIMULATED

To verify the theoretical analysis, MATLAB SIMULINK simulation and prototype experiment are both built. The simulated waveforms and experimental results of the proposed converter operating in the step-down and step-up mode are presented and discussed in the following subsections.

F. Simulated Verification

Simulations of the proposed converter in the step-down and step-up mode are obtained from MATLAB SIMULINK simulation to verify theoretical analysis preliminarily. The design of the inductors and capacitors are based on (20), (22), (24) and (26). The variations of currents through the inductors are set to 0.25, the variations of voltages across the capacitor C and C0 are set to 2% and 1%, respectively .Detailed parameters of the components are presented in Table II.

Fig. 6 shows the key time-domain waveforms in the step- down mode. In Fig. 6(a), the inductor currents iL1, iL2 and the PWM signal vg are presented. This subfigure verifies that the converter operates in CCM. In addition, the average currents of iL1 and i L2 are 0.53A and 1.78A, which are equal to the theoretical values calculated from (11) and (12), respectively. Fig. 6 (b) displays the voltage vC and the output voltage v0 along with the PWM signal vg. The average voltages of vC and v0 are

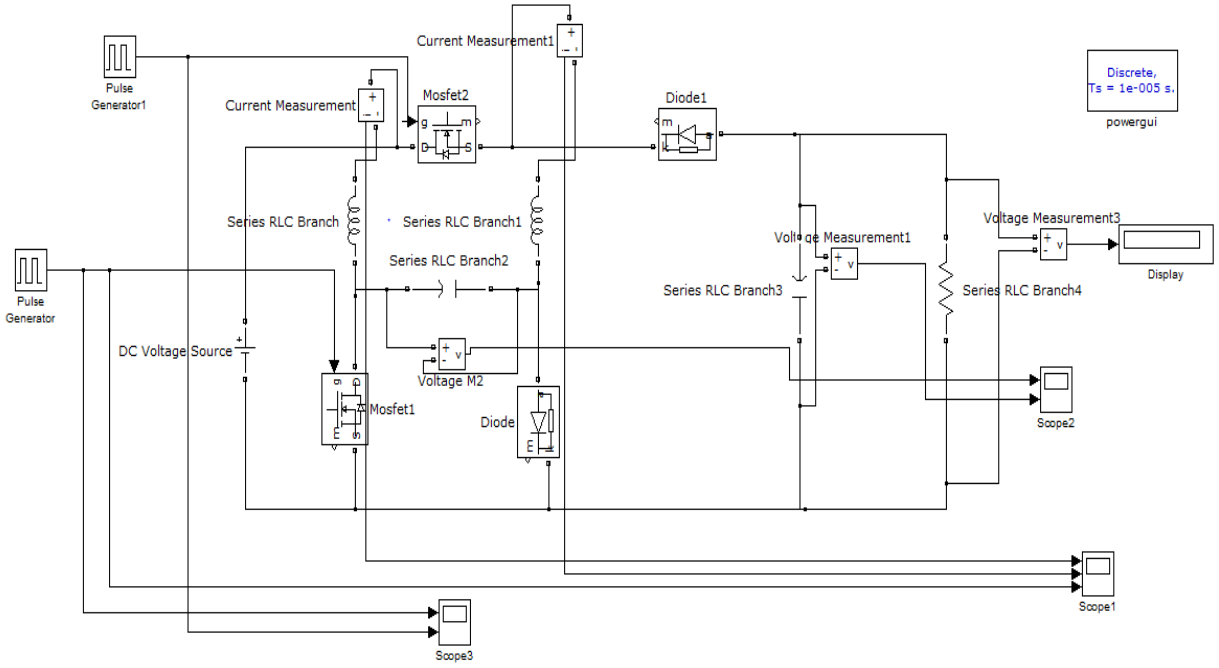


Table 2

Parameters of main circuit

Parameter	Step-Down Mode	Step-Up Mode
Input voltage V_{in}	20V	20V
Output Voltage V_0	-13.7V	-35.6V
Switching Frequency f	40kHz	40kHz
Output Load R	10Ohm	60Ohm
Duty cycle D	0.23	0.4
Inductor L_1	0.8mH	0.8mH
Inductor L_2	1mH	1mH
Capacitor C	10 µF	10 µF
Capacitor C_0	44 µF	44 µF

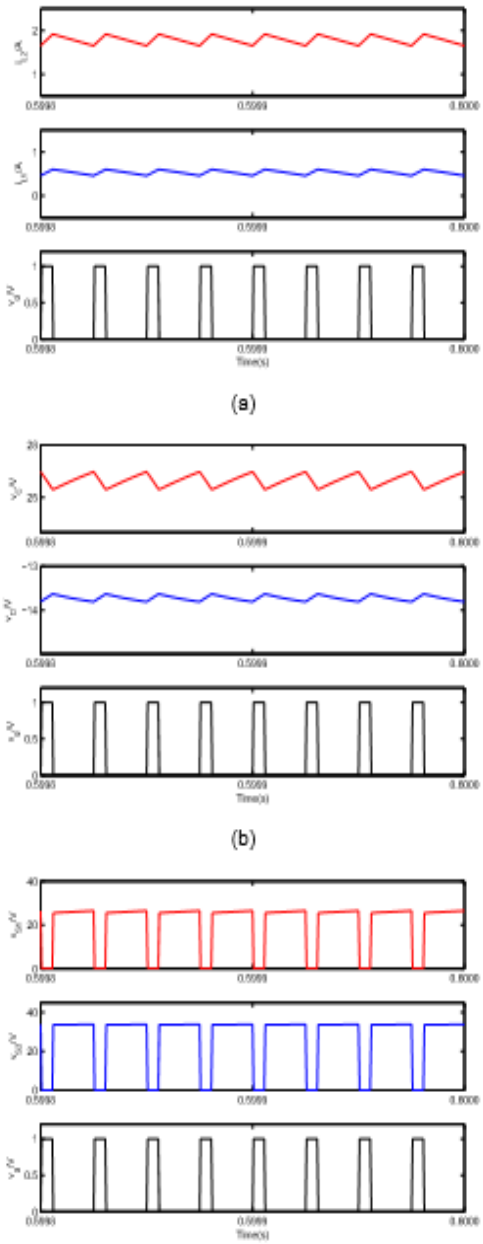


Fig. 6. Simulated waveforms of the proposed converter in step-down mode (a) i_{L2}, i_{L1} and v_g; (b) v_C, v_0 and v_g, (c) v_{S1}, v_{S2} and v_g.

26V and -13.7V, respectively, which are in good agreement with theoretical calculations from the expressions (4) and (5). Finally, the voltage stresses on power switches S1 and S2 are described in Fig. 6(c), which satisfy (9) and (10). Similar to the step-down mode, Fig. 7 presents the corresponding key waveforms in step-up mode. From Fig.7(a), the average currents iL1 and iL2 operating in CCM are 0.66A and 0.99A, respectively. From Fig.7(b), the average voltages vC and v0 are 33.3V and -35.6V, respectively. From Fig. 7(c), the voltage stresses vS1 and vS2 are 33.3V and 55.6V. All these simulated results are also coincide with theoretical calculations from the corresponding equations ((11), (12), (4), (5), (9), (10)).

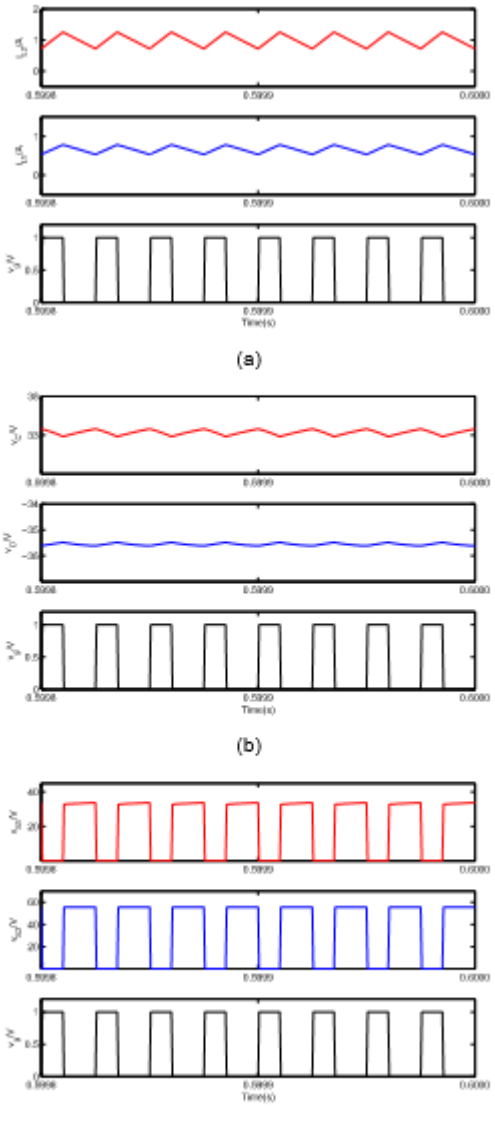


Fig. 7. Simulated waveforms of the proposed converter in step-down mode (a) i_{L2}, i_{L1} and v_g; (b) v_C, v_o and v_g, (c) v_{S1}, v_{S2} and v_g.

VI. CONCLUSION

A new negative output buck-boost converter is proposed, analyzed and validated in this paper. The detailed steady state theoretical analysis and comparisons with other N/O converters are introduced. Small signal model is established and verified by the simulations for further dynamical behaviors analysis and system design. The power losses are analyzed for calculating the efficiency. The results from the theoretical calculations, the simulations and experiments are in agreement with each other, and show that the proposed converter has no current spike and can achieve a wider range of negative output voltage. Thus, the proposed converter can provide a considerable alternative for industrial applications which need wide range of negative output voltage.

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