International Journal of Technical Innovation in Modern Engineering & Science (IJTIMES)
Impact Factor: 5.22 (SJIF-2017),e-ISSN:2455-2585
International Conference on
Recent Explorations in Science, Engineering And Technology (ICRESET'19)
Volume-5, Special Issue-March, 2019.

Application Dependent fault Diagnosis of FPGA for Low power Reconfigurable Systems

Vellingiri.A[1] Shanmuga Priya[2]

Department of Electronics and Communication Engineering
KGiSL Institute of Technology, Coimbatore, India

***Abstract*: Application-dependent test and diagnosis of FPGAs plays a very critical role in such defect tolerance scheme. This work is complementary to application-independent detection methods for FPGAs. This technique can uniquely identify any single bridging, open, or stuck-at fault in the interconnect as well as any single functional fault, a fault resulting a change in the truth table of a function, in the logic blocks. The number of test configurations for interconnect diagnosis is logarithmic to the size of the mapped design.**

The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time. Experimental results on ISCAS'89 benchmark circuits show up to 65% and 55% reductions in average and peak power, respectively.

***INDEX TERMS*—Fault diagnosis, field-programmable gate array (FPGA), testing. Built-in self test (BIST).**

I. INTRODUCTION

SRAM based field-programmable gate arrays(FPGAs) are 2-arrays of configurable logic blocks(CLBs) and have a more programmable switch matrices, surrounded by programmable input/output blocks on the periphery. FPGAs are widely used in many applications such as networking, storage systems, communication, and adaptive computing, due to their re-programmability, flexibility, and reduced time-to-market.

The re-programmability of FPGAs results in faster design and debug cycle compared to application-specific integrated circuits (ASICs). However, once the design is finalized and fixed, the programmability becomes useless and costly if infield further customization and re-programmability are not required. This is why FPGAs are very costly for high volume fixed designs with no further modifications compared to ASICs. Nevertheless, the reconfigurability of FPGAs can be readily exploited for *defect tolerance* at the manufacturing level as well as *fault tolerance* for user applications.

II. PREVIOUS WORK

Test and diagnosis of FPGAs can be categorized into *application-independent* and *application-dependent* methods. Application independent approaches target faults in the entire FPGA to ensure functionality of the device for any possible user configurations. In contrast, application-dependent techniques test and diagnose the FPGA resources with respect to a particular application mapped into the FPGA device.

III. INTERCONNECT DIAGNOSIS

The interconnect resources in FPGAs can be categorized as *inter-CLB* and *intra-CLB* resources. Inter-CLB routing resources provide interconnections among CLBs. Inter-CLB resources include programmable switch blocks and wiring channels connecting switch blocks and CLBs. Intra-CLB re-sources are located inside each CLB. Intra-CLB interconnects include programmable multiplexers and wires inside CLBs. Diagnosing faults in inter-CLB routing resources is addressed

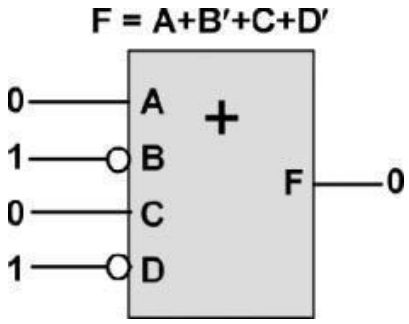

Fig. 1. Single-term function with activating input pattern.

in this section. For inter-CLB interconnect test and diagnosis, the configuration of routing resources remains unchanged while the configuration of logic resources is modified. Test and di-agnosis of intra-CLB interconnects along with logic resources are discussed in Section IV. For this purpose, the configuration of used logic resources (inclusive of intra-CLB interconnects) is kept unchanged whereas the configuration of inter-CLB interconnects as well as unused logic resources are changed.

The separation between inter-CLB and intra-CLB is made because in contemporary FPGAs the programmable logic re-sources are not limited to lookup tables (LUTs); other logic re-sources such as carry generation/propagation logic and cascade chains are included in CLBs. For inter-CLB interconnect test and diagnosis, these logic elements, if used in the original con-figuration, will be bypassed. This is discussed in the following subsections in details. It should be noted that the main focus of this paper is diagnosis of faults in island-style FPGA cores. Testing and diagnosis of embedded cores is outside the scope of this paper. Moreover, testing and diagnosis of interconnect resources directly connected to those embedded cores falls within the scope of system-on-chip (SoC) testing and can be addressed with the implementation of proper test wrappers around those blocks.

IV.BIT SWAPPING LFSR (BS-LFSR)

The proposed BS-LFSR for test-per-scan BISTs is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

Definition: Two cells in an n-bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e., without an intervening XOR gate).

Lemma 1: Each cell in a maximal-length n-stage LFSR (internal or external) will produce a number of transitions equal to 2^{n-1} after going through a sequence of 2^n clock cycles. *Proof:* The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an m-sequence. Each bit within the LFSR will follow the same m-sequence with a one-time-step delay. The m-sequence generated by an LFSR of length n has a periodicity of $2^n - 1$. It is a well-known standard property of an m-sequence of length n that the total number of runs of consecutive occurrences of the same binary digit is 2^{n-1} .The beginning of each run is marked by a transition between 0 and 1; therefore, the total number of transitions for each stage of the 2^{n-1}. This lemma can be proved by using the toggle property of the XOR gates used in the feedback of the LFSR

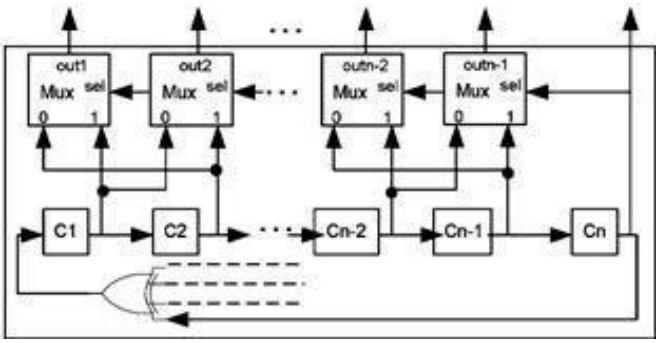

Fig. 2. BS-LFSR can be used to generate exhaustive patterns for test-per-clock BIST.

Lemma 2: Consider a maximal-length n-stage internal or external LFSR (n > 2). We choose one of the cells and swap its value with its adjacent cell if the current value of a third cell in the LFSR is 0 (or 1) and leave the cells unswapped if the third cell has a value of 1 (or 0). Fig. 1 shows this arrangement for an external LFSR (the same is valid for an internal LFSR). In this arrangement, the output of the two cells will have its transition count reduced by Tsaved = $2^{(n-2)}$ transitions. Since the two cells originally produce $2 \times 2^{n-1}$ transitions, then the resulting percentage saving is Tsaved% = 25%.In Lemma 2, the total percentage of transition savings after swapping is 25% [19]. In the case where cell x is not directly linked to cell m or cell m + 1 through an XOR gate, each of the cells has the same share of savings (i.e., 25%).Lemmas 3-10 show the special cases where the cell that drives the selection line is linked to one of the swapped cells through an XOR gate. In these configurations, a single cell can save 50% transitions that were originally produced by an LFSR cell. Lemma 3 and its proof are given; other lemmas can be proved in the same way.

Lemma 3: For an external n-bit maximal-length LFSR that implements' the prime polynomial $x^n + x + 1$ as shown in Fig. 10, if the first two cells (c1 and c2) have been chosen for swapping and cell n as a selection line, then o2 (the output of MUX2) will produce a total transition savings of 2^{n-2} compared to the number of transitions produced by each LFSR cell, while o1 has no savings (i.e., the savings in transitions is concentrated in one multiplexer output, which means that o2 will save 50% of the original transitions produced by each LFSR cell).

Proof: There are eight possible combinations for the initial state of the cells c1, c2, and cn. If we then consider all possible values of the following state, we have two possible combinations (not eight, because the value of c2 in the next state is determined by the value of c1 in the present state; also, the value of c1 in the next state is determined by "c1xor cn" in the present state).

V. CONCLUSION

In this paper, application-dependent diagnosis techniques for faults in the interconnects and logic blocks of an arbitrary design mapped into an FPGA are presented. For interconnect diagnosis, multiple faults (open, stuck-at, or bridging fault) can be uniquely identified. For logic block diagnosis, a BISD approach is presented in which multiple faults can be uniquely identified in only one test configuration. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak power is substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible.

REFERENCES

[1] I. G. Harris and R. Tessier, "Interconnect testing in cluster-based FGPA architectures," in *Proc. Des. Autom. Conf.*, 2000, pp. 49-54.

[2] G. Harris and R. Tessier, "Diagnosis of interconnect faults in cluster-based FPGA architectures," in *Proc. Int. Conf.Comput.-Aided Des.*, 2000, pp. 472-475.

[3] S. Mitra, P. P. Shirvani, and E. J. McCluskey, "Fault location in FPGA-based reconfigurable systems," in *Proc. IEEE Int. High Level Design Validation Test Workshop*, 1998, pp. 12-14.

[4] C. Stroud and M. Abramovici, "BIST-Based diagnosis of FPGA inter-Connect," in *Proc. Int. Test Conf.*, 2002, pp. 618-627.

[5] C. Stroud, S. Wijesuriya, C. Hamilton, and M. Abramovici, "Built-in self-test of FPGA interconnect," in *Proc. Int. Test Conf.*, 1998, pp.404-411.

[6] C. Stroud, E. Lee, and M. Abramovici, "BIST based diagnostics of FPGA logic blocks," in *Proc. Int. Test Conf*, 1997, pp.539-547.

[7] C. Stroud, S. Konala, C. Ping, and M. Abramovici, "Built-in self-test of logic blocks in FPGAs (Finally, a free lunch: Bist without overhead!)," in *Proc. VLSI Test Symp.*, 1996, pp. 387-392.

[8] M. B. Tahoori, "Application dependent testing of FPGAs," *IEEE Trans. Very Large Scale Integr. (VLSI) Circuits*, vol. 14, no. 9, pp. 1024-1033, Sep. 2006.

[9] M. B. Tahoori, "Application dependent diagnosis of FPGAs," in *Proc. Int. Test Conf.*, 2004, pp. 645-654.

[10] M. B. Tahoori, "Application dependent testing of FPGA interconnects,"in *Proc. Defect Fault Toler. VLSI*, 2003, pp. 409-416.