International Journal of Technical Innovation in Modern Engineering & Science (IJTIMES)
e-ISSN: 2455-2585
Volume 8, Issue 10, October-2022

Meticulous Analysis of Three-Phase Active T-Type NPC Inverter

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Abstract

In this project paper T-Type Neutral Point Clamped inverter are explained. This project is about design and implementation of three phase active T-Type NPC inverter. In this project control topology of T-Type NPC inverter using pulse width modulation technique like fixed PWM, space vector PWM and carrier based modulation technique involving sine triangular comparison like Phase disposition PWM, Alternate Phase opposition disposition PWM and Phase opposition disposition PWM are discussed. According to direction of load current at zero potential instant, corresponding switch should be turned on in order to get desired path for flow of current. This topology also describes that voltage stress across the switches reduces in OFF state. Sine PWM method is used in order to reduce the harmonics. In the enda three phase active T-Type NPC inverter is build with the help of MATLAB/Simulink in order to prove the feasibility of control method and feasibility of T-Type topology. From the satisfactory results of simulation hardware of Three Phase Active T-Type NPC inverter is built.

Keywords: T-Type Neutral, T-Type NPC inverter, PWM, Malab

Received: 7/10/2022, Accepted:17/10/2022, Published: 30/10/2022

1.1 Introduction

Multi-level converters (MLC) have been traditionally adopted for static power conversion and motor drives in medium voltage applications [1] [2]. Although various converter topologies have been developed for medium voltage applications, the three-level neutral-point clamped (NPC) converter topology is the most frequently selected for industrial applications due to its advantages of simplicity and reliability [3] [4] [5]. With the advances of modularized power devices developed for the implementation of active T-type NPC inverters [6] [7] [8] [9], AT-NPC inverters are becoming a competitive choice for PV inverters and motor drives in low voltage applications [10].

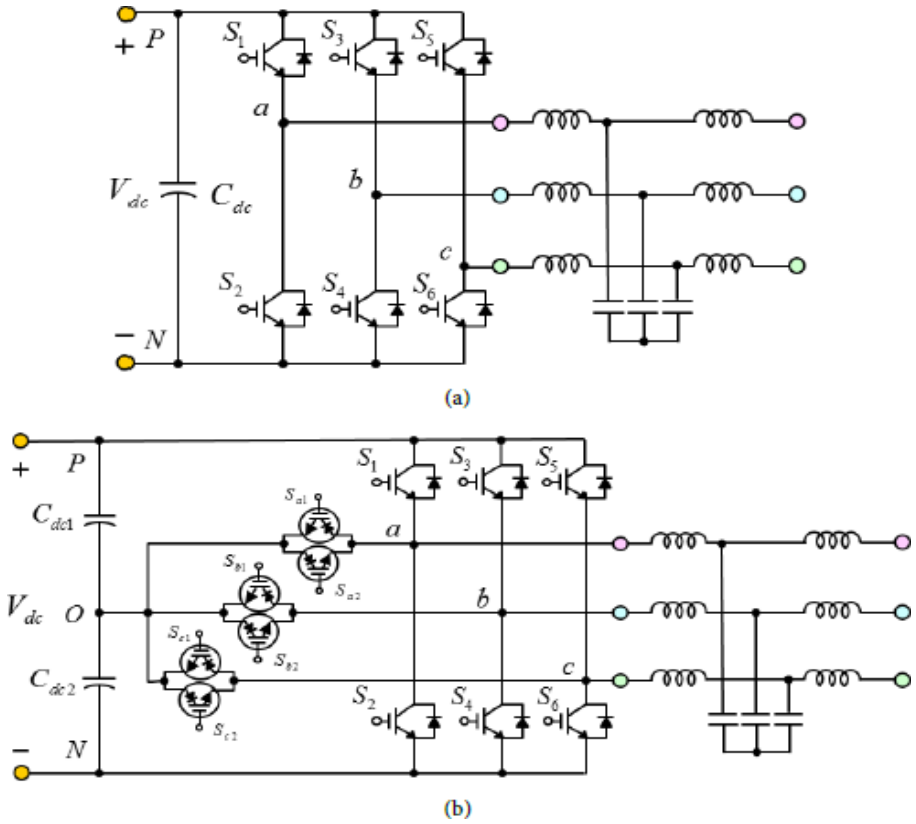

Figure 1.Schematics of (a) 2-L and (b) 3-L active T-type NPC inverters

1.2 T-Type NPC Inverter

The 3-level active T-type NPC inverter, as show in Figure 1(b), provides an additional middle point of its DC-link voltage for its voltage switching, and thus the inverter voltage is reduced to half compared with the conventional 2-level inverter as shown in Figure 1(a). The reduction of voltage switching level provides advantages such as lower switching losses, smaller filters for both the dc-link capacitor and output filters, lower EMI and leakage current, higher power density with improved efficiency. The drawbacks of the AT-NPC inverters are extra AC switches with their corresponding isolated gate drives are required, more sophisticated PWM strategy and balancing control scheme are required. However, with the development of new generation wide bandgap (WBG) semiconductors such as Gallium Nitride (GaN) and Silicon Carbide (SiC), and the high-performance advanced FPGA embedded microprocessors, an active T-type inverter phase leg may become a standard power module for the implementation of an idea renewable power conversion system.

2. Modulation Technique for Multilevel Inverter

2.1 Introduction

The main objective of the PWM is to control the inverter output voltage and to reduce the harmonic content in the output voltage. PWM techniques are most efficient techniques mainly used to provide a steady state output in terms of AC voltages irrespective of the load that makes inverter more conventional than other inverters.

There are many PWM techniques available but the most basic PWM is the sinusoidal-PWM (SPWM). The high frequency carrier wave is compared with the sinusoidal modulating signals to generate suitable gate signals for the inverters. An inverter generates an output of AC voltages from an input of DC with the help of switching circuit to reproduce a sine wave by generating one or more square pulses of voltage per half cycle.

The main advantage of PWM is that power loss in the switching devices is very low. When a switch is off there is practically no current, and when it is on and power is being transferred to the load, there is almost no voltage drop across the switch.

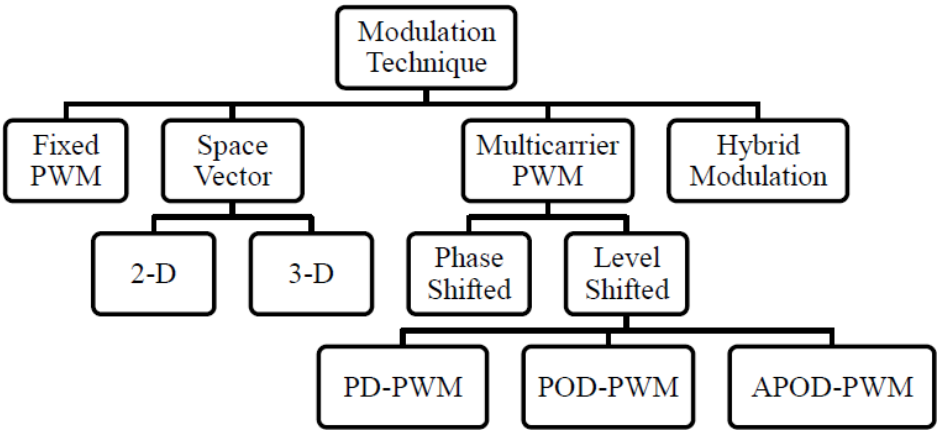

Figure 2.Modulation Techniques for Multilevel Inverter

2.2 Fixed Pulse Width Modulation

All the proposed techniques have the common property that the switching frequency is constant. As stated above this may ease the implementation of digital controllers, which often are synchronized to the switching of the inverter, which in turn is controlled by the PWM unit. Having excluded the switching frequency as the parameter to randomize, it seems that the pulse position is the only quantity which can be randomized while still keeping the average voltage produced by the inverter fully controllable within each switching interval.

However, as discussed shortly this is not the case. The fundamental idea behind random pulse position techniques is that the mean voltage measured across one switching interval is independent of the position of the pulse. This degree of freedom may be utilized in various ways, and from a theoretical point of view, the only constraint is that a pulse must not extend beyond the boundaries of the switching interval in question. That constraint may be met in a number of different ways, but the literature dealing with random pulse position has focussed almost exclusively on one simple variant, namely the so called lead-lag random pulse position technique originating.

2.3 Space Vector Pulse Width Modulation

Among various modulation techniques for a multilevel inverter, space vector pulse width

modulation (SVPWM) is an attractive candidate due to the following merits. It directly uses the control variable given by the control system and identifies. Each switching vector as a point in complex (α, β) space. It is suitable for digital signal processor (DSP) implementation.
It can optimize switching sequences. The space vector diagram of any three-phase n-level inverter consists of six sectors. Each sector consists of (n − 1)2 triangles. The tip of the reference vector can be located within any triangle. Each vertex of any triangle represents a switching vector. A switching vector represents one or more switching states depending on its location.

There are n3 switching states in the space vector diagram of an n-level inverter. The SVPWM is performed by suitably selecting and executing the switching States of the triangle for the respective on-times. It is known as "Nearest Three Vector" (NTV) approach. The performance of the inverter significantly depends on the selection of these switching states.
Figure 2 shows the space vector diagram of a three-level inverter. There are six sectors (S1−S6), four triangles (0−3) in a sector, and a total of 27 switching states in this space vector diagram. As level n increases, the increased number of triangles, switching states, and calculation of on-times adds to the complexity of SVPWM for multilevel inverters.

2.4 Carrier Based Sine Triangular Pulse Width Modulation

Carrier based Sine Triangular PWM technique involves a high frequency triangular as carrier wave and a Sine wave which has frequency equal to fundamental frequency. By comparing both these waves pulses are obtained for the switches. To operate a multilevel inverter, Multicarrier Sine Triangular PWM technique is used. It has more than one carrier wave and one reference wave. There are several types of Carrier based Sine Triangular PWM techniques which are classified as follows.

2.4.1 Phase Disposition Pulse Width Modulation

In phase disposition pulse width modulation (PDPWM) strategy, all the carrier waves are in phase with each other. The reference and carrier waveform arrangement for phase disposition pulse width modulation is shown in Figure 3

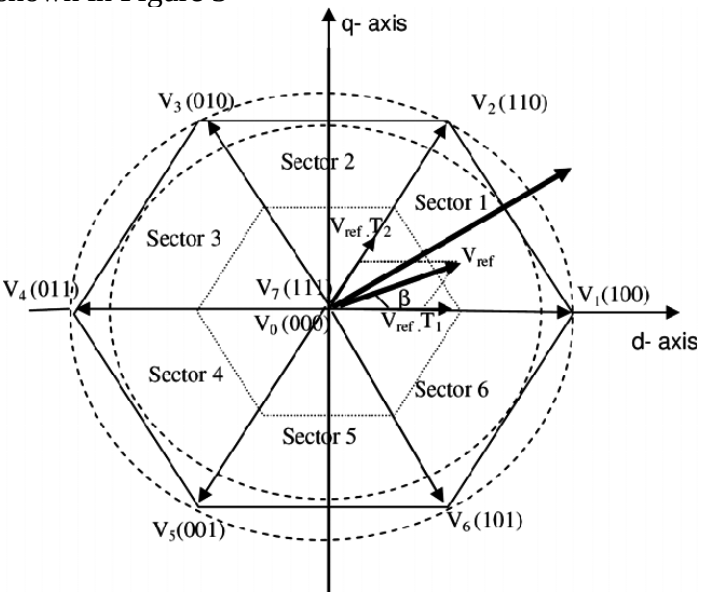

Figure 3.Space Vector PWM Technique

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As shown in figure 4, The gate pulses for the switches S1, S2, S3 and S4 are generated using the PDPWM technique, The gate pulses for the switch used for Positive voltage are generated by comparing sine wave with upper triangular carrier wave, and the Gate Pulses for the switches used for Negative voltage are generated by comparing the same sine wave to the lower triangular carrier wave.

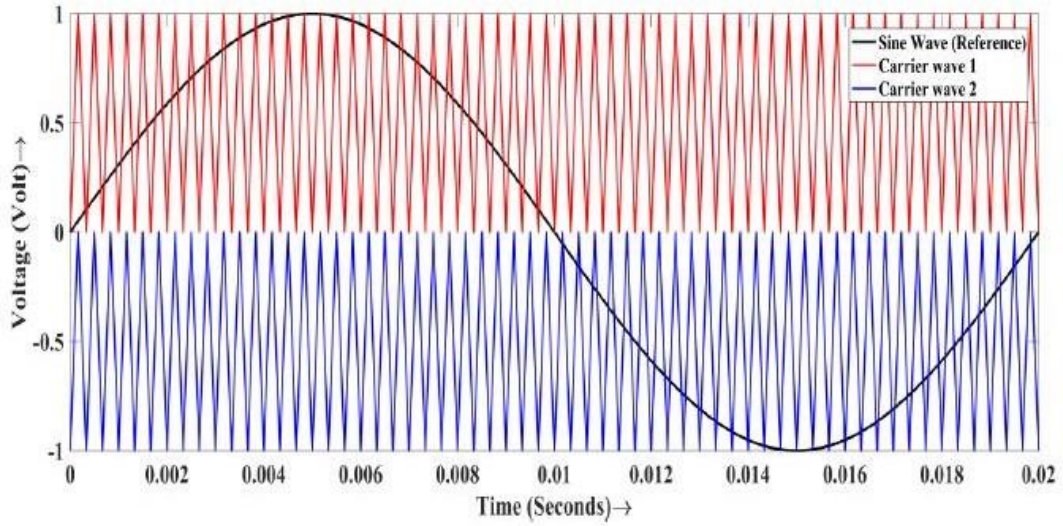

Figure 4.Phase Disposition Pulse Width Modulation

2.4.2 Alternate Phase Opposition Disposition Pulse Width Modulation

In Alternative phase opposition disposition pulse width modulation (APODPWM) strategy, where each carrier is phase shifted by 180 from its adjacent carrier wave. The reference and carrier wave arrangement for alternate phase opposition disposition pulse width modulation is shown in figure 5.

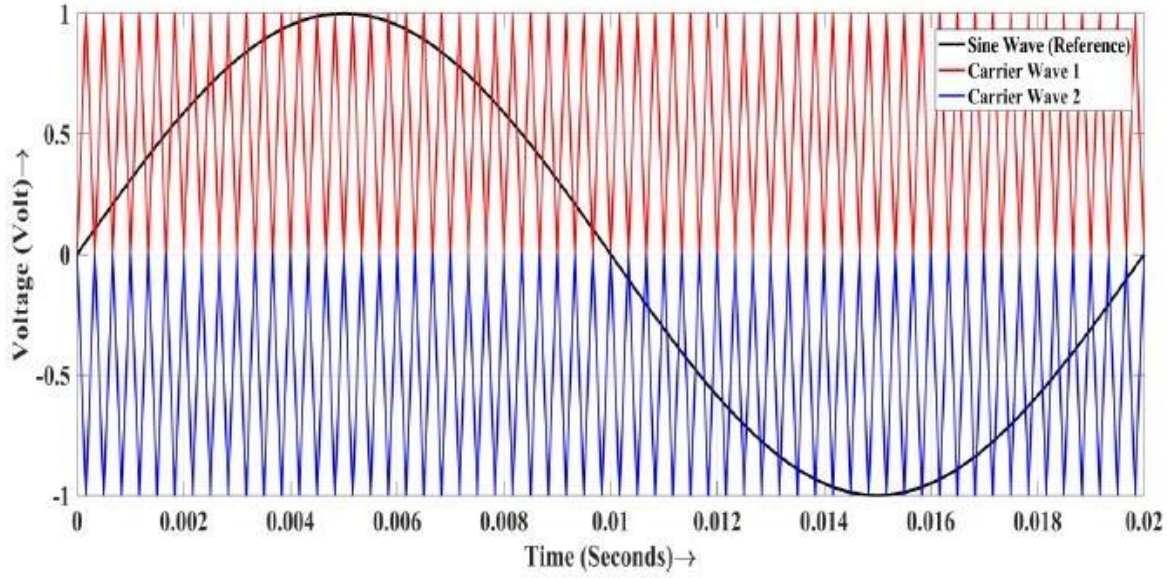

Figure 5.Alternate Phase Opposition Disposition

The gate pulses for the switches S1, S2, S3 and S4 are generated using the APODPWM

technique, The gate pulses for the switch used for Positive voltage are generated by comparing sine wave with upper triangular carrier wave, and the Gate Pulses for the switches used for Negative voltage are generated by comparing the same sine wave to the lower triangular carrier wave.

2.4.3 Phase Opposition Disposition Pulse Width Modulation

In phase opposition disposition pulse width modulation (PODPWM) strategy, has all the carrier waveforms above zero reference to be in phase with each other and those below the zero reference to be 180 out of phase from the carrier wave above zero reference. The reference and carrier waveform arrangement for phase opposition disposition pulse width modulation is shown in figure 6. PODPWM technique is used in this project. As this strategy is complicated than PDPWM strategy but experiments have shows that half wave as well as quarter wave symmetry is obtained using this strategy only. In PDPWM technique, at the time of zero crossing instant of reference wave, during positive half cycle the reference wave and carrier wave both have magnitude equal to zero, but at the zero crossing instant of negative half cycle, carrier wave has its maximum vale while reference wave has magnitude equal to zero. This leads to loss of half wave symmetry and quarter wave symmetry. Half wave symmetry and quarter wave symmetry can be obtained easily by PODPWM technique.

As shown in figure 6, The gate pulses for the switches S1, S2, S3 and S4 are generated using the PODPWM technique, The gate pulses for the switch used for Positive voltage are generated by comparing sine wave with upper triangular carrier wave, and the Gate Pulses for the switches used for Negative voltage are generated by comparing the same sine wave to the lower triangular carrier wave.

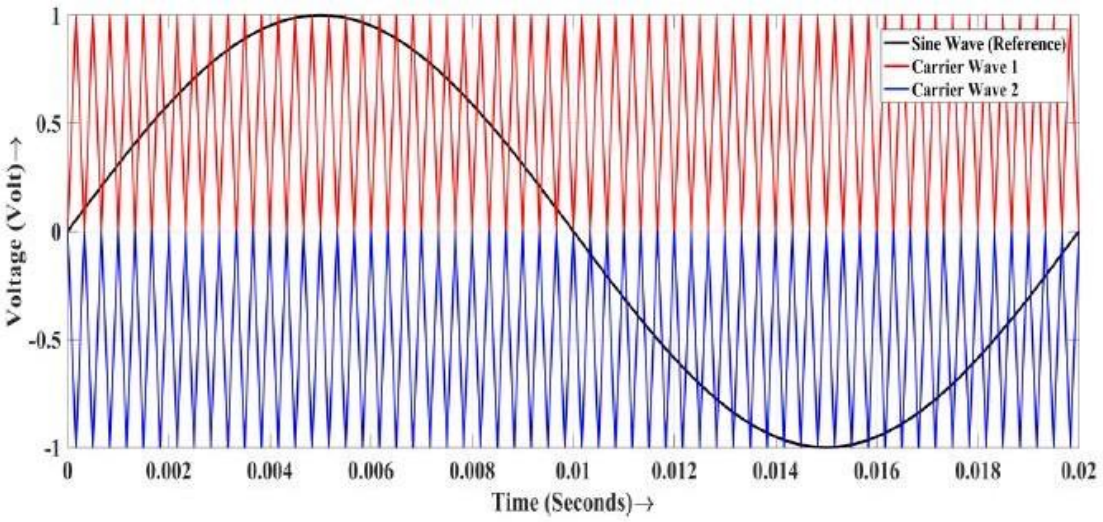

Figure 6.Phase Opposition Disposition

3. Simulation and hardware results and discussion

- **Pulse Generator**

It contains Gate pulse generator of all switches. It has triangular blocks and function generator generating three phase reference sine waves. A single sine wave and two triangular waves are compared using comparator block and gate pulses are obtained.

- **Inverter**

It contains three phase Active T-Type NPC Inverter. It also contains a DC link having two DC sources of 500 Volt each connected in series.

- **Three Phase Series RLC load**

This block contains three phase series RLC load consuming 500 KVA at a power factor of 0.75 lagging.

Parameter	Rating
Sample Rate	$50e^{-6}$ Second
Simulation Time	0.06 Second
Carrier 1 Amplitude	1 Volt
Carrier 2 Amplitude	1 Volt
Carrier Frequency	3000 Hertz
Fundamental Frequency	50 Hertz
DC Source 1	500 Volt
DC Source 2	500 Volt
DC Link Voltage	1000 Volt
KVA Rating of Load	500 KVA
Load Power factor	0.75 (Lag)
Line Voltage	1000 Volt
Line Current	460 Ampere

Figure 7.Simulation Parameter

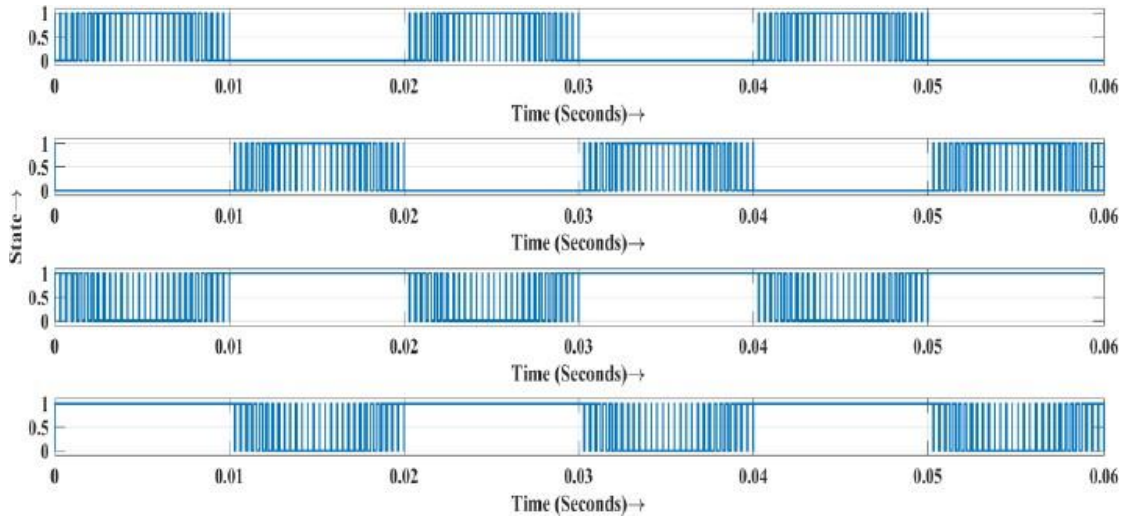

Figure 8.Gate Pulse

Figure 8 shows the gate pulses for the switches of one phase. It is observed that there is half wave and quarter wave symmetry in the output as explained in PODPWM. First two pulses are for main switches and last two pulses are for auxiliary switches.

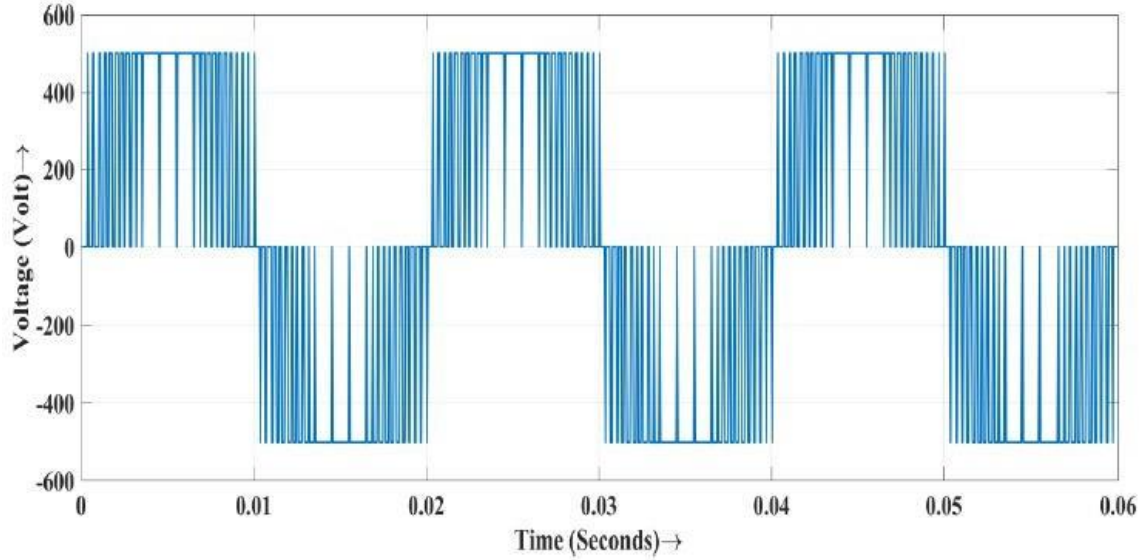

Figure 9.Pole Voltage

Figure 9 Shows the Pole Voltage of one of the three phases. Here peal value is 500 Volt. Half wave symmetry and quarter wave symmetry obtained in the Gate Pulses is reflected on the output side as well in spite of low carrier frequency.

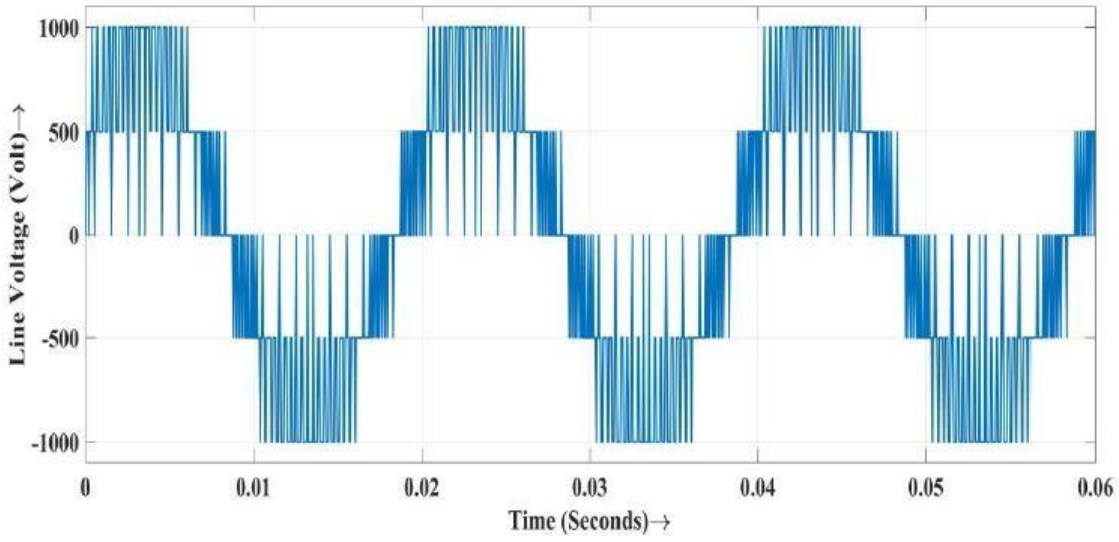

Figure 10.Line Voltage

Figure 10 shows Line Voltage. Here peal value is 1000 Volt. Here also half wave symmetry as well as quarter wave symmetry is obtained.

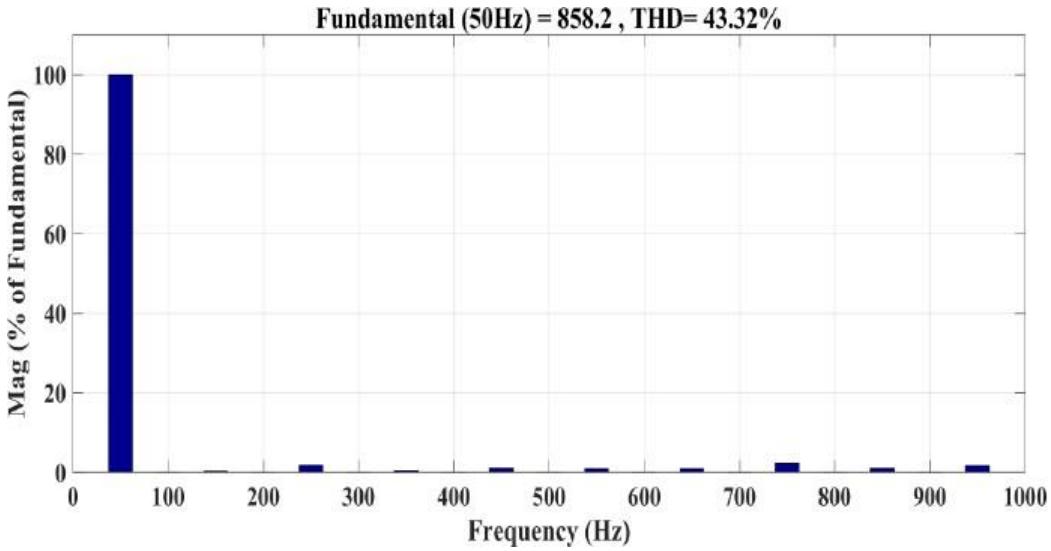

Figure 11.FFT Analysis of Line Voltage

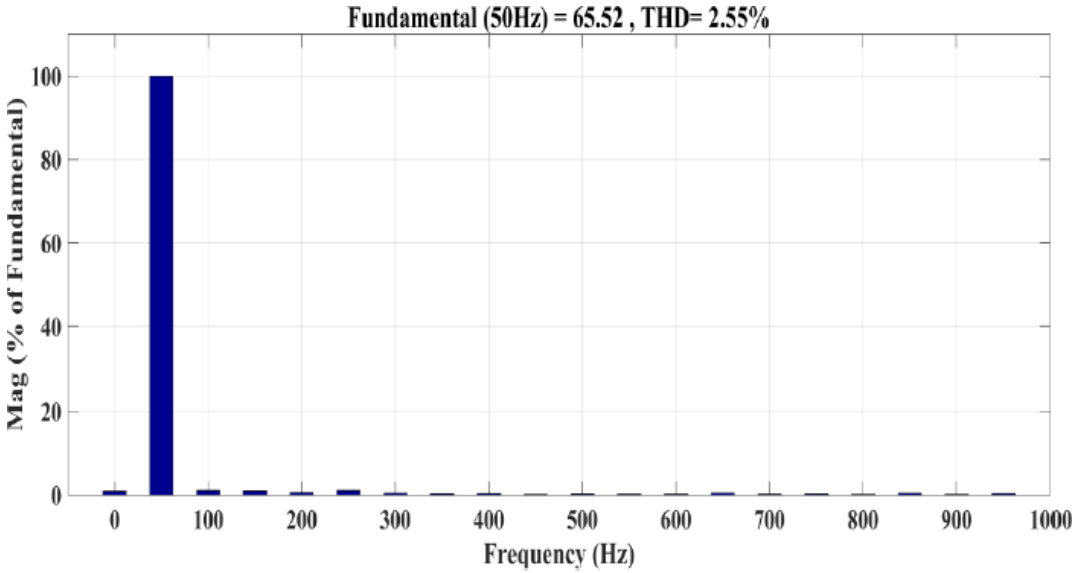

Figure 12.FFT Analysis of Line Current

Figure 11 shows the FFT analysis of Line Voltage. %THD is the Line Voltage is 43.32%. But every individual harmonic distortion is less than 5% and their order is also quite high. It is easy to remove them from the system with the help of harmonic filters. Figure 12 shows FFT analysis of Line Current. %THD in Line Current is 2.55%. This value
is within the limits given by IEEE and IEC.

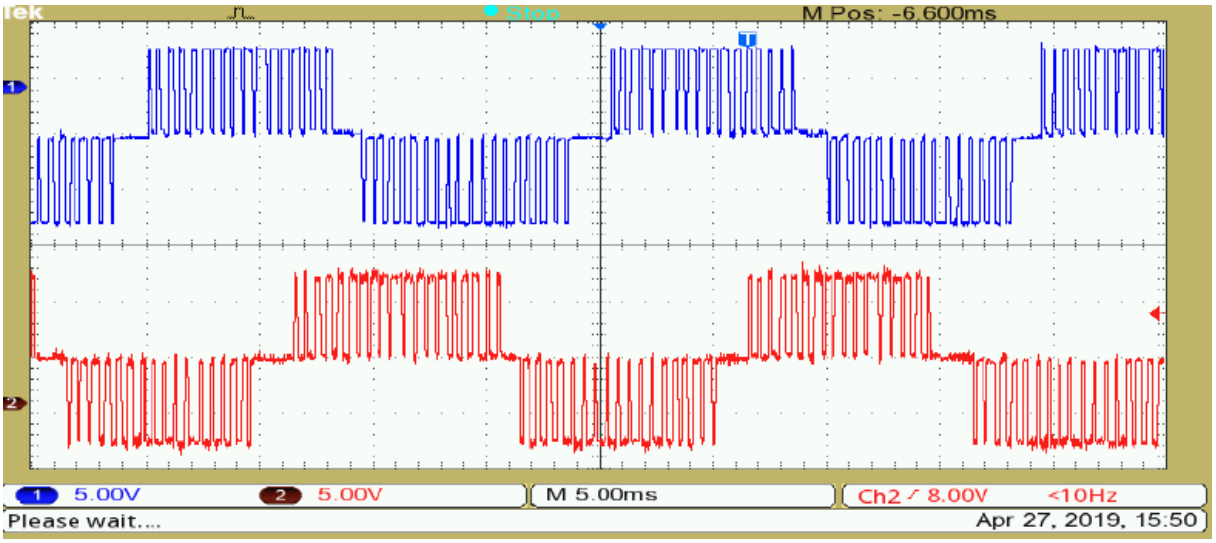

Figure 13.Pole Voltage

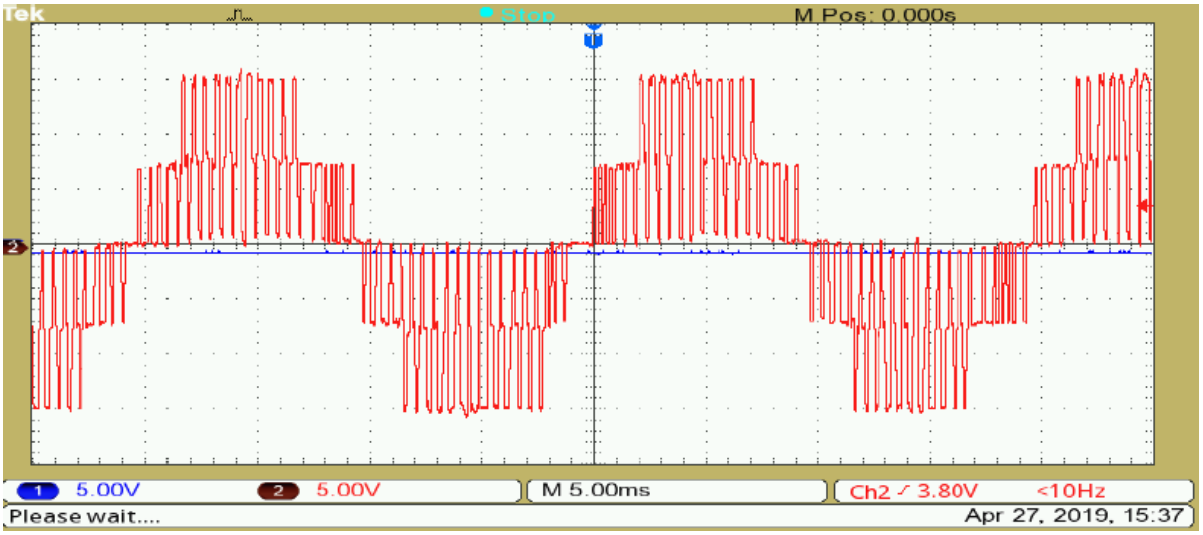

Figure 14.Line Voltage

Figure 13 shows the pole voltage obtained from the inverter. Here it is clearly observed that the experimental results are same as simulated results. Here half wave as well as quarter wave symmetry is maintained. Figure 14 shows the line voltage obtained from the hardware. Here also the results are same as simulated results.

Conclusion

Now a days power generation from renewable sources in increasing rapidly. The power generated from the solar panels is DC power. Power consumption in today's era is in the form of AC power. There is a gap between power generated (DC) and power consumed (AC) which is filled by Inverter. The design of electrical machines is such that they require

sinusoidal voltage and current to operate satisfactorily. In the conversion from DC to AC via two level inverter sinusoidal wave shape of voltage is not obtained. Here comes Multilevel Inverter into the picture. With the help of Multilevel Inverter, a staircase voltage can be obtained. As the levels of an inverter are increased, the similarity of voltage obtained to the sinusoidal wave shape is also increased. Diode clamped Inverter, Flying Capacitor inverter and Cascaded H-Bridge inverter along with three phase active T-Type neutral point clamped are explained in this report. Diode clamped inverters have been obsoleted from the system due to their inefficient operation and no control over neutral point clamping. Flying capacitor inverters are also not used these days because of requirement of large capacitor banks.

Cascaded H-Bridge inverter were popular in past but due requirement of isolated DC source, they are being removed from the system and replaced by T-Type NPC inverters. It is observed that T-Type NPC inverters have fewer switches, they do not need large capacitor banks and they have control over each operation with an efficient operation. Modulation techniques for multilevel inverter are also explained in this report. Carrier based Sine Triangular PWM is widely used technique. With the help of proper modulation technique, harmonics can be reduced significantly using same hardware. Harmonics leads to losses and less efficient operation. Proper modulation technique improves efficiency significantly.

PODPWM is used in this project. With the help of this technique, harmonics in the current are reduced to 2.55% for a load having power factor of 0.75 lagging. A simulation is built with the help of MATLAB/Simulink. In the end hardware of the three phase active T-Type NPC inverter is made. It is observed from the results that output of the Inverter is same as simulated inverter.

References

1. Nabae, A., Takahashi, I. and Akagi, H. (1981) A New Neutral-Point-Clamped PWM Inverter. IEEE Trans. Ind. Appl., 17, 518-523. https://doi.org/10.1109/TIA.1981.4503992
2. Franquelo, L.G., Rodriguez, J., Leon, J.I., Kouro, S., Portillo, R. and Prats, M.A.M. (2008) The Age of Multilevel Converters Arrives. IEEE Ind. Electron. Mag ., 2, 28-39. https://doi.org/10.1109/MIE.2008.923519
3. Rodriguez, J., Bernet, S., Wu, B., Pontt, J.O. and Kouro, S. (2007) Multi-Level Voltage- Source-Converter Topologies for Industrial Medium-Voltage Drives. IEEE Trans. Ind. Electron., 54, 2930-2945.https://doi.org/10.1109/TIE.2007.907044
4. Rodriguez, J., Bernet, S., Steimer, P.K. and Lizama, I.E. (2010) A Survey on Neutral- Point- Clamped Inverters. IEEE Trans. Ind. Electron., 57, 2219-2230. https://doi.org/10.1109/TIE.2009.2032430
5. Koutroulis, E. and Blaabjerg, F. (2013) Design Optimization of Transformerless Grid- Connected Pv Inverters Including Reliability. IEEE Trans. on Power Electronics , 28, 325-335.https://doi.org/10.1109/TPEL.2012.2198670
6. Schweizer, M., Friendly, T. and Kolar, J.W. (2013) Comparative Evaluation of Advanced Three-Phase Three-Level Inverter/Converter Topologies against Two-Level Systems. IEEE Trans. Ind. Electron., 60, 5515-5527. https://doi.org/10.1109/TIE.2012.2233698

7. Teichmann, R. and Bernet, S. (2005) A Comparison of Three-Level Converters versus Two- Level Converters for Low-Voltage Drives, Traction, and Utility Applications. IEEE Trans. onIndustry Applications , 41, 855-865. https://doi.org/10.1109/TIA.2005.847285
8. Maximilian, S., Benjamin, S. and Uwe, J. (2016) Evaluation of a NPC1 Phase Leg Built fromThree Standard IGBT Modules for 1500 VDC Photovoltaic Central Inverters Up to 800 Kva. 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 1-8.
9. Mario, S. and Johann, W.K. (2013) Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications. IEEE Trans. on Power Electronics , 28, 899-907. https://doi.org/10.1109/TPEL.2012.2203151
10. Mario, S. and Johann, W.K. (2011) High Efficiency Drive System with 3-Level TType Inverter. 14th European Conference on Power Electronics and Applications (EPE Conf. Proc.), 1-10.