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Design Low Power 1-Bit CMOS Full Adder using DG FINFET Technique

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Abstract:- This paper proposes a 1-Bit CMOS full adder cell utilizing Double Gate (DG) FINFET (Fin Shaped Field Effect Transistor). The point of this paper is to diminish spillage power and spillage current of 1-bit CMOS Full Adder while keeping up the feasible introduction with less transistors are used (transistors calculate 10). A new elevated show 1-bit CMOS Full Adder in light of new rationale scheme is displayed in this paper. DG FINFET method which diminishes the procedure minor departure from 1-bit CMOS Full Adder is actualized in this paper; the legitimization of DG FINFET system is connected on 1-bit CMOS Full Adder is to diminish leakage power and leakage current. We examine We look at the utilization of DG FINFET innovation gives low spillage and superior activity by using fast and low thresh hold voltage transistors for logic cells. 1-bit CMOS Full Adder proposed design is simulated using Cadence tool at 90nm and 45nm technology.

Key Words: CMOS, 1-bit CMOS Full Adder, Leakage Power, Leakage Current, Cadence.

1. Introduction

The batteries driven and portable devices are of a great demand in many industrial applications which need the implementation of low power and area efficient devices [1, 2]. Moore's law was discovered by Gordon Moore in 1965. He was the Co-founder of INTEL Corporation. He has set the pace for our modern digital revolution and utilized that the computing world increases in power and decreases in cost. This prediction is known as Moore's Law. Today, many of the industrial applications are designed in nanometer range. The transistor dimension is confined with the marvels like Short Channel Effects which incorporate hot bearer impact and burrowing through oxide thickness. In CPU, Airthmetic logic unit (ALU) is a critical part. The adder cell is a vital unit of an ALU. Numerous advanced circuit adders are utilized to perform expansion of numbers [3, 4]. In numerous PCs, adders are utilized in different parts of the processor to compute addresses [5], table files and comparative tasks. Due to the increase in the demand of portable devices such as mobile phones, lap top, tablets [6, 7], and the need of area and power efficient VLSI circuits is arisen. Low power adder (LPA) cells are utilized in Low power applications. In this paper, an enhanced 1-bit full adder circuit is actualized which expends decreased power and less number of transistors.

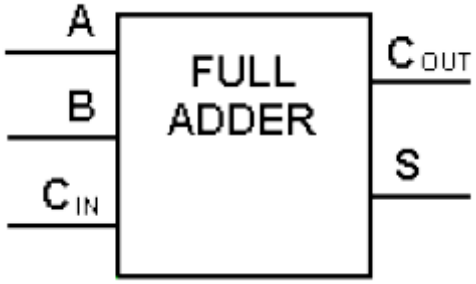

Figure.1 Block Diagram of 1-bit Full Adder

Today there are a heightening number of versatile applications A with restricted measure of intensity accessible, requiring little region, and low-power and high throughput hardware. In this way circuits which expend low power turn into the real concern factor for plan of chip and framework segments. The examination exertion in low power microelectronics has been heightened and low power VLSI frameworks have developed as exceedingly sought after. Adder is a standout amongst the most imperative parts of a CPU (focal preparing unit), ALU, and drifting point unit and address age like store or memory get to unit. Of course, extending enthusiasm for flexible sorts of apparatus Such as telephones, personal digital assistant (PDA), and Notebook PC, rise the need of using zone and Power effective VLSI circuits. Low-power and rapid snake cells are utilized in battery-task based gadgets. Thus, outline of an elite full-snake is extremely valuable and indispensable [8]. A standout amongst the most surely understood full adders is the standard CMOS full snake that utilizations 28 transistors as

appeared in Figure 2. In this paper, we present an I-bit full-snake circuit, which uses 10 transistors check with proper power use, concede execution. The fundamental preferred standpoint of 10 transistors full adders are-low region contrasted with higher door tally full adders [9], bring down power utilization, and lower working voltage. It turns out to be increasingly troublesome and even outdated to keep full voltage go in reverse and forward task as the plans with less transistor tally and lower control utilization are sought after [10]. In pass transistor rationale, the yield voltage go in reverse and forward might be de-evaluated because of the edge misfortune issue Thus, alluring its introduction is critical for improving the general module execution [11]-[12]. The essential inconvenience of the 10 transistors full adders is experiencing the limit voltage loss of the pass transistors. They all have twofold limit misfortunes in full viper yield terminals [13]. These disadvantages were defeated in this paper by applying DG FINFET system to 10 Transistor I-Bit full viper outlines.

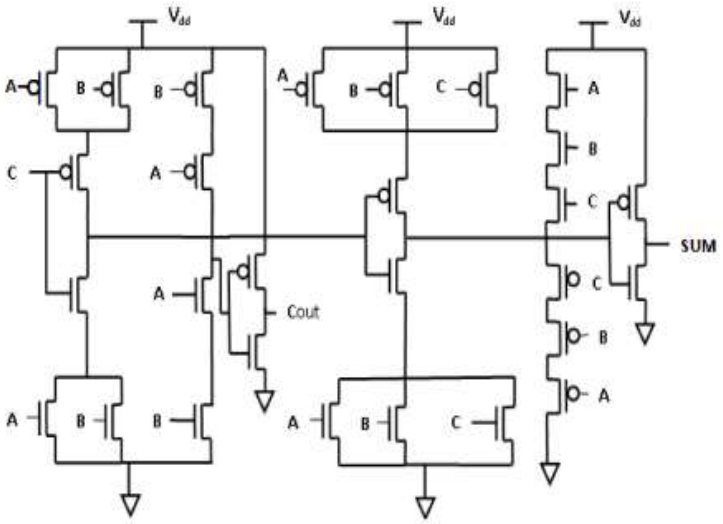

Figure.2 Schematic of conventional Full Adder

2. 1-Bit CMOS Full Adder Architecture

In this paper, we present a 1-bit CMOS full-adder circuit, with reasonable power utilization, defer execution and obligation cycle. We have reenacted a 1-bit CMOS Full-adders circuit alongside different 10 transistors and thought about the Power dispersal, proliferation delay, and different parameters. The fundamental preferred standpoint of 10 transistors CMOS full adders are-low region contrasted with higher gate check full adders, bring down power utilization, and lower working voltage. It turns out to be increasingly troublesome and even out of date to keep full voltage go in reverse and forward activity as the plans with less transistor tally and lower control utilization are sought after. The decrease in voltage swing, on one hand, is advantageous to control utilization. Then again, this may prompt moderate exchanging on account of fell activity, for example, swell convey snake. At low VDD activity, the debased yield may even reason breakdown of circuit [14]. In this manner, for plans utilizing decreased voltage swing, uncommon thought must be paid to steadiness the power utilization and the speed [15]. For the usage of different 10 transistors CMOS full adder circuits we required either 4 transistors XOR circuit or 4 transistor XNOR circuit and 2-to-I multiplexer. The schematic of 1-bit CMOS Full Adder is appeared in figure 4 and the yield waveform is appeared in Figure 5 and Leakage current waveform is appeared in Figure 6.

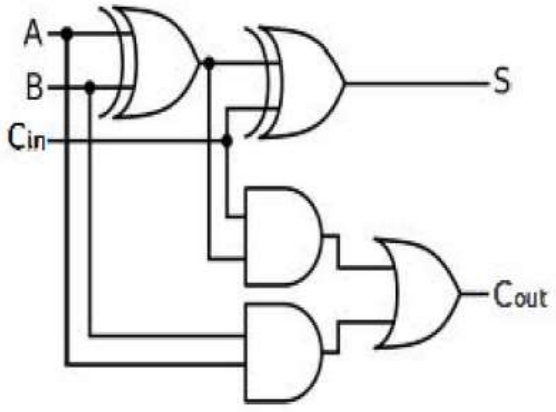

Figure.3 Gate Level Diagram of 1-bit Full Adder

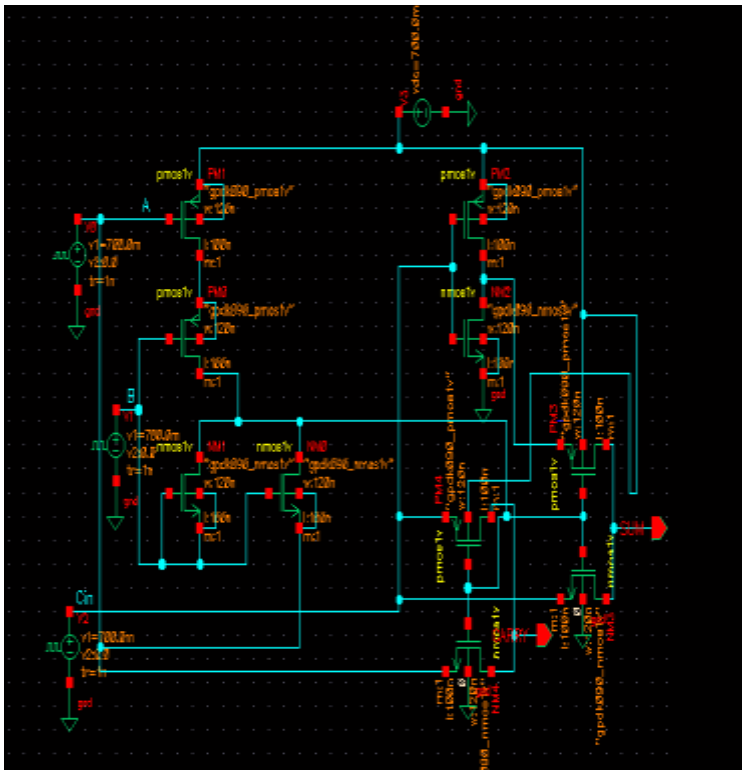

Figure.4 Schematic of 1-bit CMOS Full Adder

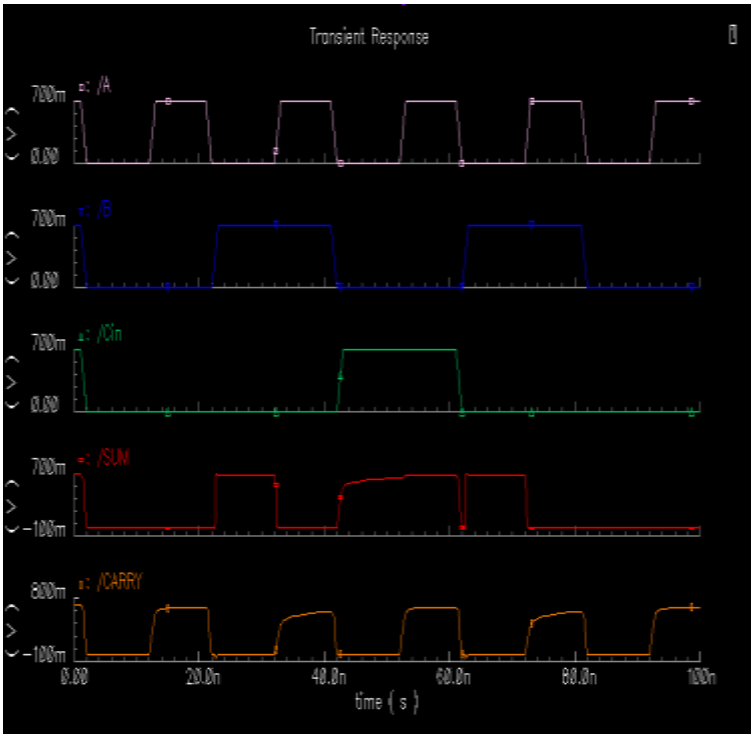

Fig.5 Transient Response of 1-bit CMOS Full Adder

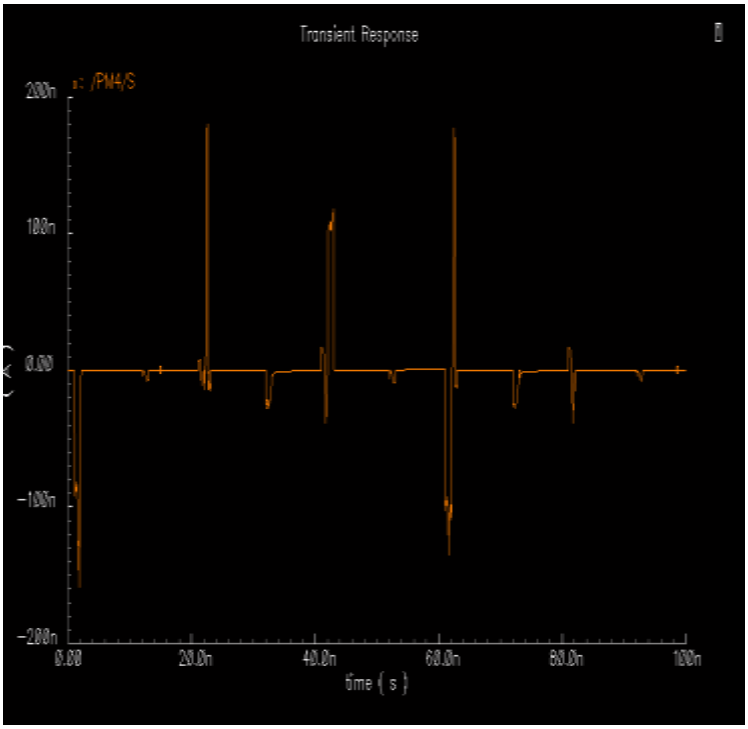

Fig.6 Leakage Current of 1-bit CMOS Full Adder

This topology utilizes an aggregate of 10 transistors for the execution of following rationale articulations. Consider a 1-bit CMOS full adder. This circuit has two operands, An and B, and an information convey, Cin. It creates the whole

$$SUM = A \oplus B \oplus Cin$$
$$CARRY = AB + BCin + ACin$$

3. 1-Bit Full Adder Using DG FINFET Technique

FINFET means Fin Field Effect Transistor. FINFET is a Non Planar Dual Gate Transistor used in the Silicon Architecture which consists of very large computational density. FINFET was instituted by Berkeley scientists of college of California and it was created for the utilization of Silicon-on-Insulator. FINFET development takes its name from the manner in which that the FET structure used takes after a course of action of cutting edges when seen. The key typical for the FINFET is that it has a main channel wrapped by a thin silicon "fin" from which it gets its name. The thickness of the balance decides the powerful channel length of the gadget.

Double gate FINFET system is connected on I-bit Full Adder cell. Here self-deciding control of front and back gate in DG FINFET can be productively used to create execution and lessen control utilization. In non-basic ways self-deciding entryway control can be utilized to combine parallel transistors. A parallel transistor match comprises of two transistors with their source and depletes terminals integrated. The second door is added inverse to the traditional entryway in Double-Gate (DG) FINFETS, which has been unsurprising for their forthcoming to predominant control short channel impacts, and in addition to control spillage current. The activities of FINFET is perceived as short gate (SG) mode with transistor doors joined together, the independent gate (IG) mode where self-deciding computerized signals are utilized to drive the two gadget doors, the low power and ideal power mode where the back gate is connected to a turnaround inclination voltage to lessen spillage control and the crossover mode, which utilizes a course of action of low power and self-deciding gate modes. In because of its base material the continuous down in scaling of mass CMOS makes key issues. The essential snags to the scaling of mass CMOS to 45nm gate lengths incorporate short channel impacts, ideal current, gate dielectric spillage, and gadget to gadget varieties. Yet, FINFET based plans offers the better command over short channel impacts, low spillage and better yield [16] in 45nm aides than beat the deterrents in scaling The schematic of DG FINFET connected on 1-bit CMOS Full Adder is appeared in figure 7. The yield waveform of 1-bit CMOS Full Adder utilizing DG FINFET method is appeared in figure 8, waveform of spillage current is appeared in figure 9 separately.

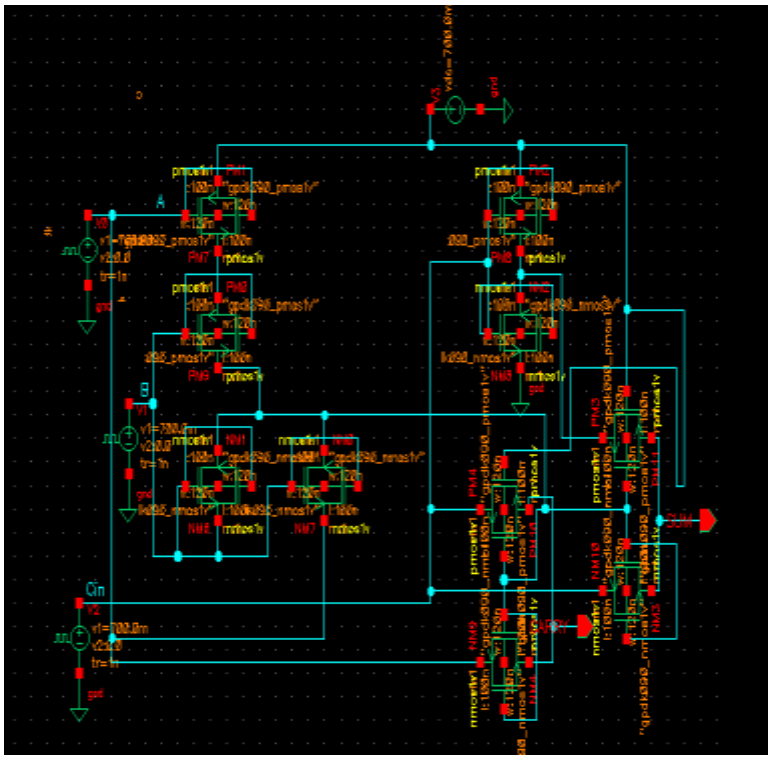

Figure.7 Schematic of 1-bit CMOS Full Adder using DG FINFET Technique

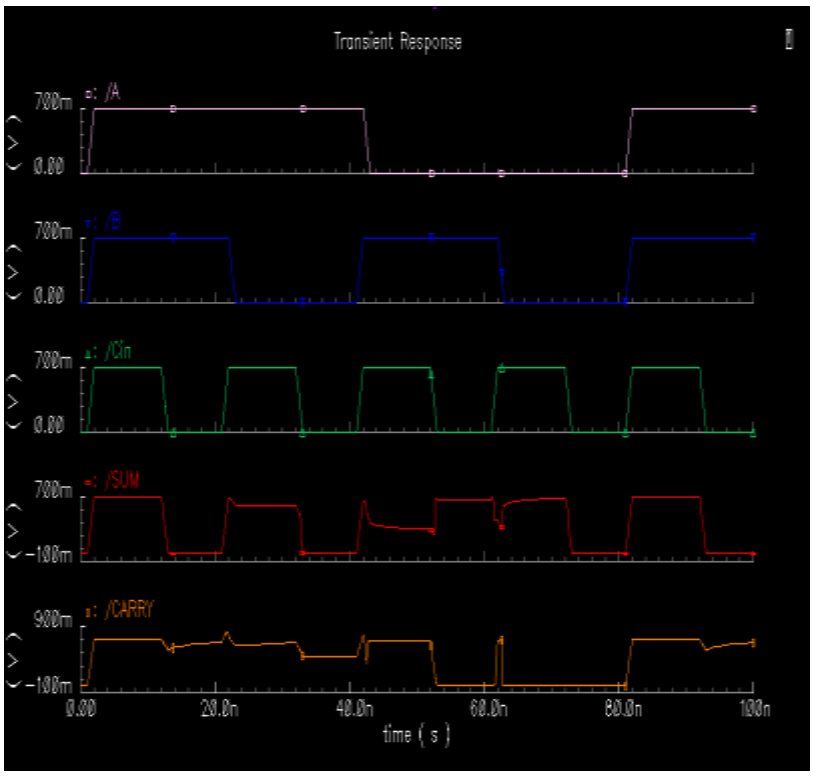

Fig.8 Transient Response of 1-bit CMOS Full Adder using DG FINFET Technique

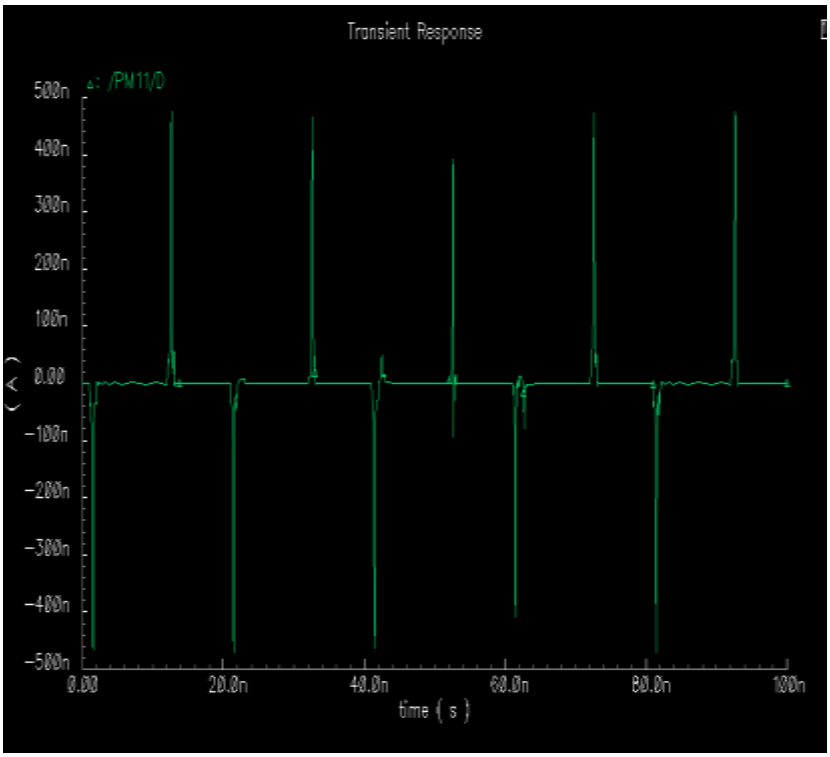

Fig.9 Leakage Current of 1-bit CMOS Full Adder using DG FINFET Technique

4. Simulation Result

1-bit CMOS Full Adder Simulation has been done on cadence tool using the 90nm and 45nm technology with a nominal supply voltage Vdd = 0.7 V. The gate leakage being the main predominant instrument at room temperature 27°C, distinct strategies have utilized for decrease of intensity utilization and keeping up the performance of 1-bit CMOS Full Adder, 1-bit CMOS Full Adder using DG FINFET technique, it compares1-bit CMOS Full Adder and 1-bit CMOS Full Adder using DG FINFET technique the parameter like Leakage Current, leakage power Graphs are shown in Figure 10 and Figure 11 respectively.

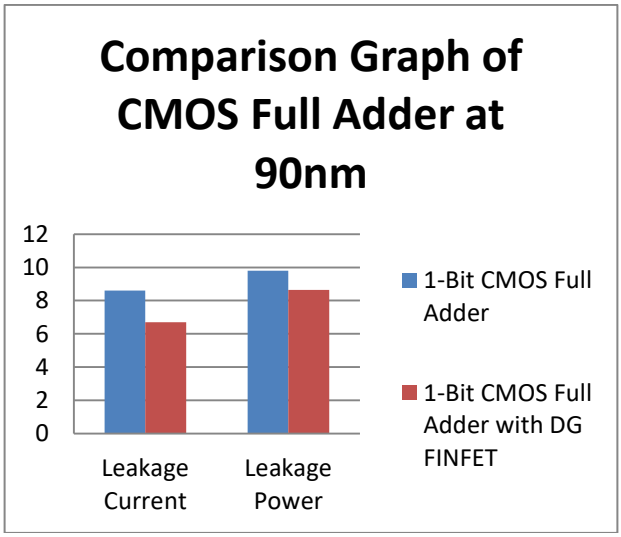

Figure.10 Comparison Graph of 1-Bit Full Adder at 90nm

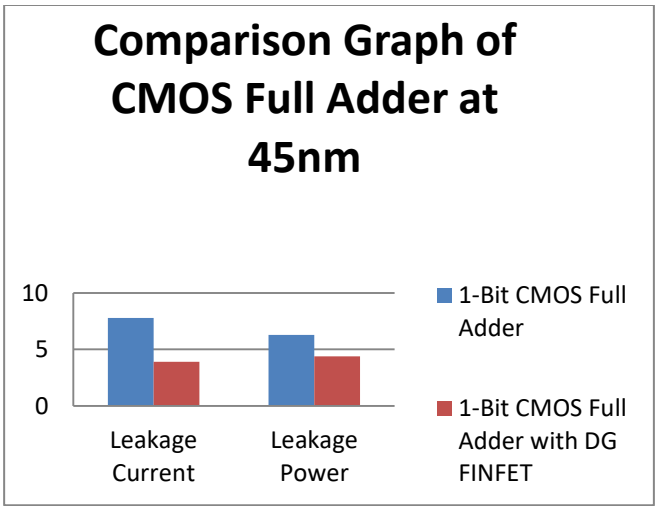

Figure.11 Comparison Graph of 1-Bit Full Adder at 45nm

Comparisons Result Summary of1-Bit CMOS Full Adder and 1-Bit CMOS Full Adder with DG FINFET is shown below table 1.

Table 1 Simulated Result Summary

Performance Parameter	1-Bit CMOS Full Adder	1-Bit CMOS Full Adder with DG FINFET	1-Bit CMOS Full Adder	1-Bit CMOS Full Adder with DG FINFET
Technology Used	90nm	90nm	45nm	45nm
Supply Voltage	0.7V	0.7V	0.7V	0.7V
Leakage Power	9.8nW	8.64nW	6.3nW	4.6nW
Leakage Current	8.6nA	6.7nA	7.8nA	3.9nA
Transistor count	10	10	10	10

Conclusion

A 1-Bit CMOS Full Adder based on DG FINFET technique has been proposed. The analysis of the recreated results affirms the possibility of the DG FINFET procedure in 1-Bit CMOS Full Adder outline and demonstrates that decrease of intensity scattering parameter when contrasted with 1-Bit CMOS Full Adder at supply voltage of 0.7V. DG FINFET 1-Bit CMOS Full Adder has a minimal increment in region contrasted with the 1-Bit CMOS Full Adder; generally speaking, we accomplished the most reduced power scattering. Simulation result is measured by CANDENCE VIRTUOSO Tool. In this paper comparative description of DG FINFET techniques have been offered on the bases of min leakage power at supply voltage Vdd=0.7 V, threshold voltage (0.35 V) and input control voltage is also 0.7V. Simulation result furnishes 1-Bit CMOS Full Adder with DG FINFET systems is superior to anything 1-Bit CMOS Full Adder.

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