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Analysis on Different Metal Strategies for Clock Tree Synthesis

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Abstract— Clock Tree Synthesis is playing a vital role in physical design, distributing clock nets to all the sync points and balancing skew and insertion delay at the same instance to meeting the time. To balance insertion delay and skew, different methods will follow like adding buffers, inverters, up sizing, down sizing cells in the clock network. For routing these clock tree also we can use different metal strategies for balancing skew and insertion delay This paper mainly analyses that how the clock tree effect for different metal strategies utilized for routing and effect on skew and insertion delay by using the tool CADENCE ENCOUNTER.

Keywords— CTS, ROUTING, STA, VLSI, PHYSICAL DESIGN.

I. INTRODUCTION

Clock Tree synthesis is playing a crucial part in VLSI. CTS is nothing but distributing or propagating clock signal to each and every sync point in that network. The main goal in this stage is to maintain skew and insertion delays as maximum as possible. We have different techniques to propagate clock like Binary tree, H Tree, X tree structurs. Up to placement stage we will propagate ideal clock that is insertion delay is zero after placement trail route will be done and we can real delays. In the routing stage we need to route clock tree with different metals and observe the results.

II. PROPERTIES NEED TO ANALYSE DURING CTS

A. Skew

In synchronous sequential circuit systems with same source of clock signal reaches at different sink points at different times, that is the variation between the reaching of any two perticular clocks is called local skew.

B. Insertion Delay

The insertion delay is nothing but latency, but latency associated with two terms clock source latency and network latency. The time consuming by the clock to reach from its initial point to clock definition point or common path for clock is called Source latency. Network latency is time consuming by the clock signal to be reached from the clock definition point to the clock pin of the sequential module.

C. Slack

Slack is nothing but the variation between required time to arrival time of data. If slack is positive means that the path is free of violation and if it is negative then path is violated

III. DIFFERENT METAL STRATEGIES FOR CTS

A. CTS Routing with M1-M2 layers

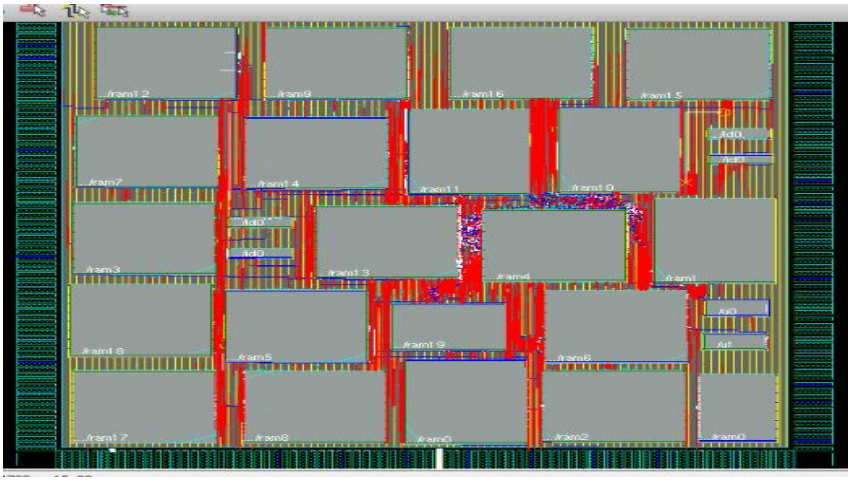

Fig. 1 CTS with M1-M2 routing layer in Cadence Encounter

The above Fig1 shows the Clock tree was generated or propagated with Metal 1 and Metal 2 . In Fig1 white coloured spots are congestion. Congestion is nothing but the requirement tracks for the routing of available tracks are very less. If we use M1 and M2 then more voltage drop will occur because of high resistance. The lower metals having high resistance due to having less width long length. Actually M1 and M2 utilized for the follow pins mean while for local power supplies. If the resistance is more delay will be more and that requires number of buffers to balance the timing. Here Table.1 shows the results that skew is very high that is unwanted. Slack also negative that means some paths are Violating.

Skew	Slack	Latency	Clock pin
0.180	-1.347	1.550	Launch flip flop clock pin
		1.370	Capture flip flop clock pin

Table. 2 Results for CTS M1 – M2 routing layer in Cadence Encounter

B. CTS Routing with M3-M4 layers

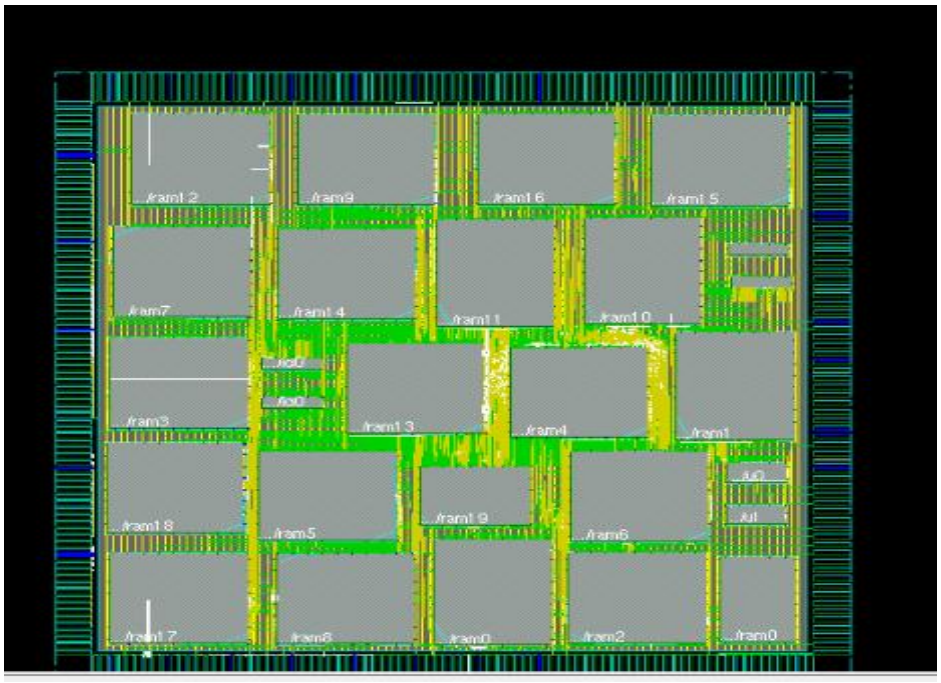

Fig. 2 CTS with M3-M4 routing layer in Cadence Encounter

The above Fig2 shows the Clock tree was generated or propagated with Metal 3 and Metal 4. If we use M3 and M4 then less voltage drop will occur because of moderate resistance. The middle metal layers having moderate resistance due to having moderate metal width. Actually M3 and M4 utilized for Clock tree generation. If the resistance is moderate delay will be moderate and that requires less number of buffers to balance the timing. Here Table.2 shows the results that skew is very less that is good. Slack also negative but compared to before it got reduced. Most of the time middle metal layers are preferred to Clock tree generation. Because middle metal layers will utilize routing resources effectively.

Skew	Slack	Latency	Clock pin
0.137	-1.349	1.565	Launch flip flop clock pin
		1.428	Capture flip flop clock pin

Table. 2 Results for CTS M3 – M4 routing layer in Cadence Encounter

D. CTS Routing with M5-M6 layers

The below Fig3 shows the Clock tree was generated or propagated with Metal 5 and Metal 6 . If we use M5 and M6 then less voltage drop compare to M3 and M4 metals. This metal layers having low resistance due to having higher metal width. Actually M5 and M6 utilized for critical nets where we need less voltage drop. If the resistance is low the corresponding delay will be low and that requires few buffers to balance the timing. Here Table.3 shows the results that skew is little bit increased because these metal layers are having high metal width. If more metal width means occupying more tracks and that leads to congestion. If congestion is more the routing nets uses long paths to routing.

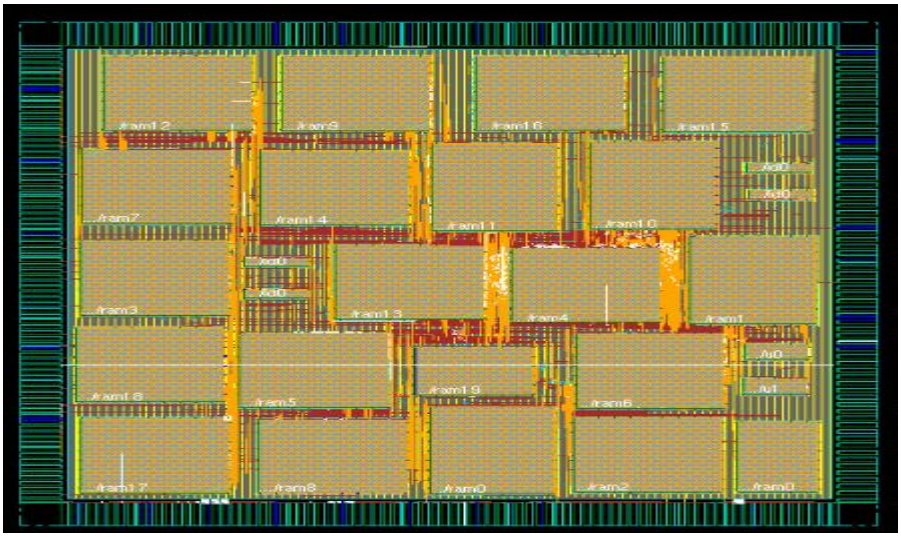

Fig. 3 CTS with M5-M6 routing layer in Cadence Encounter

Slack also more negative that results requirement of buffers will be more as shown in Table.3 below. Most of the higher metal layers are preferred to routing the critical nets. Because M5 and M6 metal layers will utilize routing resources unnecessarily.

Skew	Slack	Latency	Clock pin
0.166	-1.556	1.402	Launch flip flop clock pin
		1.236	Capture flip flop clock pin

Table. 3 Results for CTS M5 – M6 routing layer in Cadence Encounter

E. CTS Routing with M6-M7 layers

The below Fig4 shows the Clock tree was generated or propagated with Metal 6 and Metal 7 . If we use M6 and M7 then very less voltage drop compare to all metals before used. This metal layers having low resistance due to having higher metal width. Actually M6 and M7 utilized for power routing to avoid voltage drop.

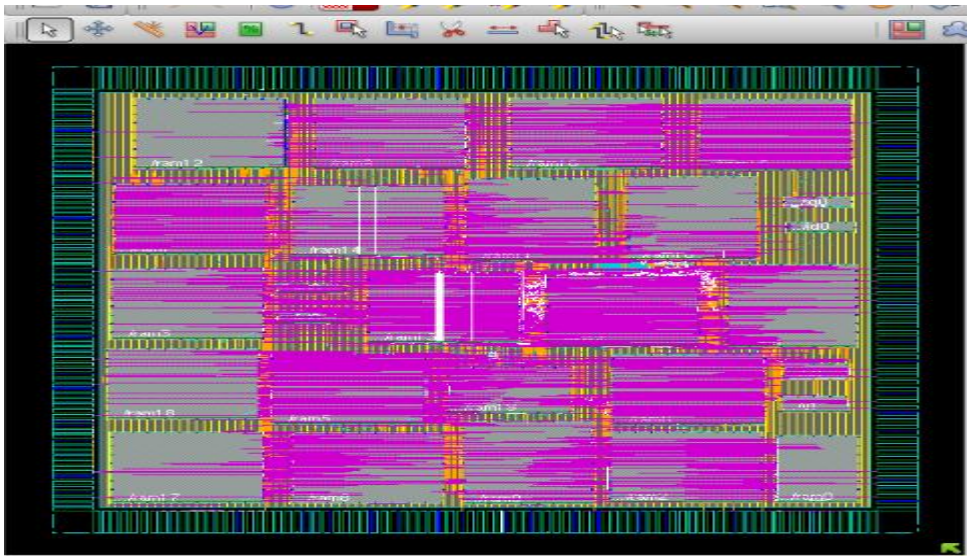

Fig. 4 CTS with M6-M7 routing layer in Cadence Encounter

If the resistance is very low the corresponding delay will be low and that requires very less buffers to balance the timing. Here Table.4 shows the results that skew decreases because these metal layers are having high metal width.

If more metal width means occupying more tracks and that leads to congestion. If congestion is more the routing nets uses long paths to routing. That is why here we are seeing slack also more negative that results requirement of buffers will be more. Most of the higher metal layers are preferred to routing the power nets. Because M6 and M7 metal layers will utilize routing resources unnecessarily. Now we can observe more congestion.

Skew	Slack	Latency	Clock pin
0.150	-1.513	1.376	Launch flip flop clock pin
		1.226	Capture flip flop clock pin

Table. 4 Results for CTS M6 – M7 routing layer in Cadence Encounter

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IV. CONCLUSIONS

By analyzing all results we can suggest that middle metal layers are more preferable for clock tree generation. That will give us less skew and less slack. If slack and skew is less that requires few buffers only. The utilization of chip area also more effective. For optimization also it will consume less time.

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