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Analysis of Instrumentation Amplifier at 180nm technology

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Abstract— Instrumentation amplifier are used in ECG, EMG and it is required that they produce a stable and noise free output. This research paper shows the design of instrumentation amplifier using two-stage Miller op-amp. CMRR is increase upto 92dB which is enough to suppress DC offset or noise to a great extent. Along with this phase margin and gain are also improved in the proposed circuit. The proposed design has been able to satisfy most of the specifications needed for the INA. The entire design has been done in 180 nm technology using cadence tool

Keywords— INA, ECG, CMRR, Miller

I. Introduction

Electroencephalogram (EEG) and EMG (Electromyogram) respectively are electrical signals resulting from the human brain activity and from contraction/ relaxation of body muscles. Traditionally, these signals are acquired using electrodes and amplified using instrumentation amplifiers. Acquisition of these signals is done differentially while any common mode component of the bio-potential is rejected. This is very essential because the required bio-potentials are typically weak signals with low voltage levels where as the likely common mode signals that are coupled with the bio-potentials are much larger in amplitude. For instance, in EKG acquisition, signal amplitudes are typically in microvolt range with maximum values about 0.5mV. A 60Hz interference signal from the supply mains is typically coupled to the differential electrodes and thus appears as a common signal which is much larger in voltage compared to the desired EKG signal. This signal is referred to as a common mode signal and has to be rejected whereas the differential EKG signals is acquired. The ability of an instrumentation amplifier to amplify required differential signals while rejecting unwanted common mode signals is quantified by its Common Mode Rejection Ratio (CMRR). Instrumentation amplifier properties vary depending on its topology and application. The most common instrumentation amplifier is the 3 – Op-amp instrumentation amplifier. This topology though is not suitable for portable bio-potential signal monitoring since it demands high power consumption and has very poor CMRR. The poor CMRR of the 3- Op-amp IA is due to the use of passive components in its feedback network. So, here design of proposed INA replaces the resistors with the capacitors. Also, two-stage op-amp is used to build the whole circuitry instead of conventional op-amp.

Operational amplifiers are one of the most popular elements in nearly all electronic systems. Hence designing an efficient Op-amp has become a major need. Various research works are being done to achieve reliable and stable results. Apart from stability and reliability, other parameters such as speed, power, gain, bandwidth, noise etc also plays a vital role in designing the Op-amp. Hence, designing of any Op-amp can be a challenging task. It is often observed a trade off between power and bandwidth so Op-amp should be made according to the requirements of any application. Operational amplifiers are one widely used building blocks in mixed signal systems and analog applications too. Therefore, it is essential that output of Op-amps must be stable and should be noise free. Stability of Op-amp is a major concern as if the output is not stable then the results will not be efficient and it keeps on oscillating. Design analysis of any Op-amp is based on the requirements of any circuit. In a single stage Op-amp, hence stability is quite less in any circuit. Therefore according to the need in nowadays applications, two stage Op-amps has become a major need and if the design approach of two-stage Op-amp is correct then cascading designs can also be implemented. It can give high output swing and high gain and thus proves to be important for advanced CMOS technologies. Basic block diagram showing the three stages of of a two stage Op-amp is shown in Fig. 1

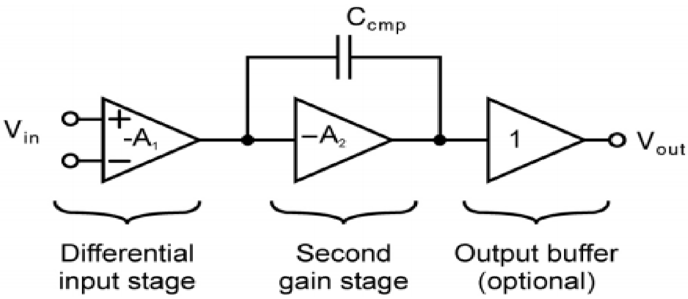

Fig. 1 Block diagram of a Two-stage Op-amp

Gain margin is another design parameter and it should always be greater than 1 for better stability. Gain margin acts as a safety factor for model uncertainty. In simple words, Gain margin describes that particular amount of gain which gets increased or decreased doesn't affect the stability of the circuit. Phase and gain margin should both be high for better results.

II. CONVENTIONAL INA

INA is composed of three op-amps. The inpust are applied to both the op-amps in input stage and output of both the op-amps are fed to a differential amplifier as shown in Fig. 2. Schematic shown in Fig. 2 is composed of differential op-amp which is shown in Fig. 3. This conventional INA is used in less number of applications because of less gain and phase

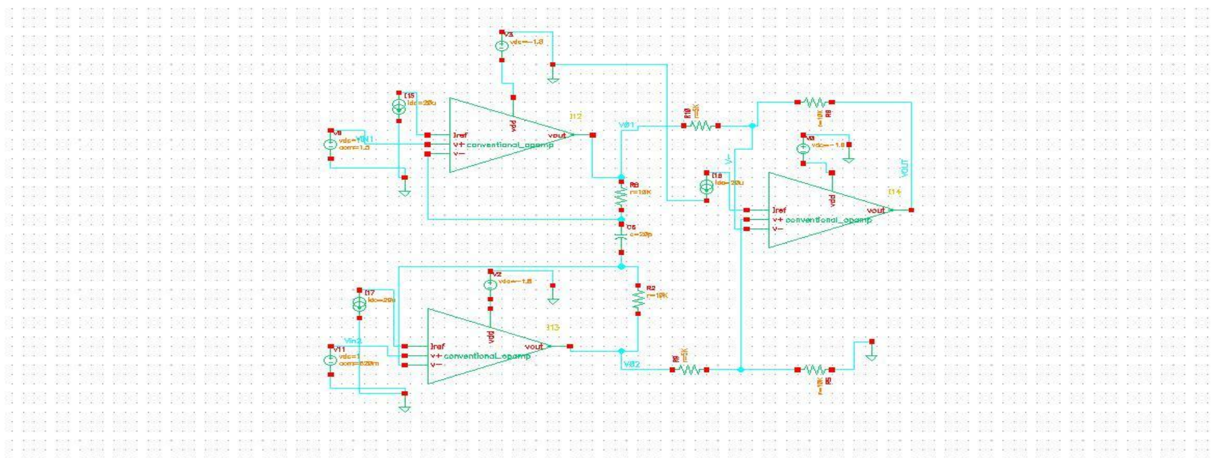

Fig. 2 Schematic of Conventional INA

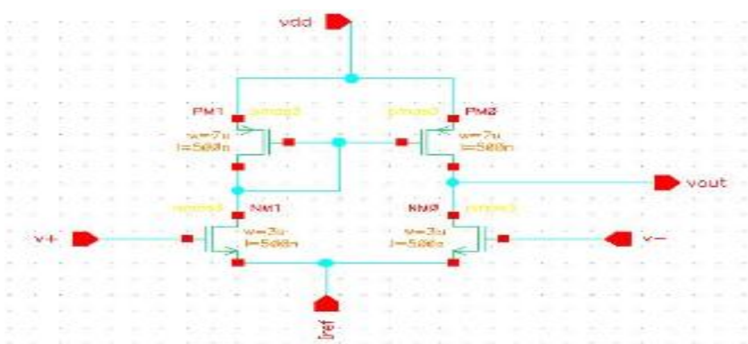

Fig. 3 Schematic of Differential op-amp

II PROPOSED INA USING TWO-STAGE MILLER OP-AMP

Instrumentation amplifier can be implemented using single stage or two-stage Op-amp. As two stage op-amp shows high gain and phase margin as compared to the single stage op-amp Therefore, instead of using conventional Op-amp, Fig. 4 shows the schematic of INA using two stage Miller op-amp Fig. 5

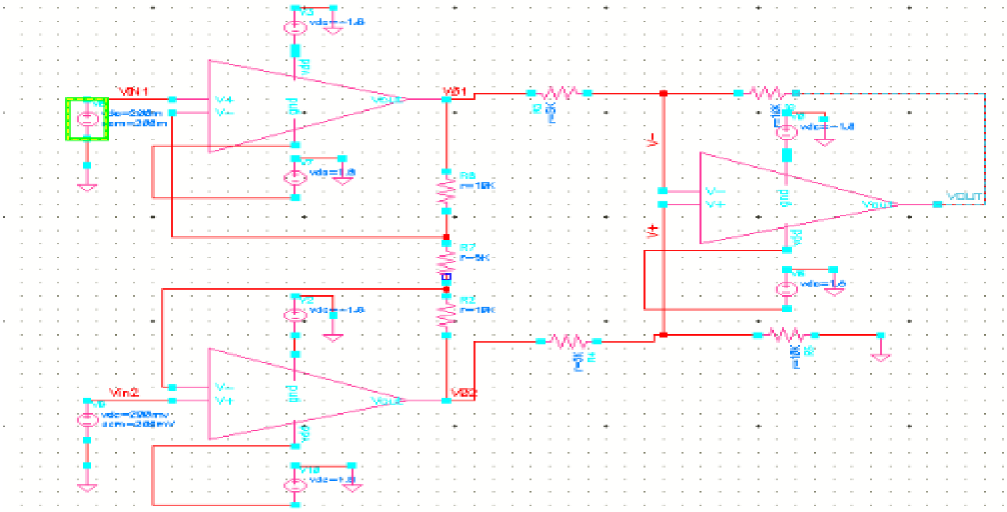

Fig. 4 Schematic of Modified INA

A. *CMRR Calculations of Modified INA*

Common mode rejection ratio (CMRR) and common mode rejection (CMR) measure the ability of a differential input amplifier, such as op-amp or an INA, to reject signals common to both inputs. In other words, as the common-mode voltage differs from how it is specified in the data sheet, an offset voltage appears at the input.This offset voltage is in addition to the initial input offset voltage and also amplified by the differential gain of the device or circuit. So, the ability of device to suppress such signals is the measure of CMRR. CMRR is calculated as-

CMRR = AD/AC and in dB it is calculated as

$$CMRR = 20\log(AD/AC) \qquad 1$$

Where AD and AC are the differential and common mode gain.

$$AD = Vo/\ Vid \qquad 2$$

Where Vid = (Vin1 -Vin2)

Vid = (200-150)mV = 50mV

As Vin1 = 200mV and Vin2 = 150mV

For Vo simulation is performed and resultant waveform is shown in Fig. 6

AD=Vo/Vid, Vo=1.68V from the waveform

Now putting the values of Vo and Aid in equation 2

AD= 1.68V/50mV

=33.6

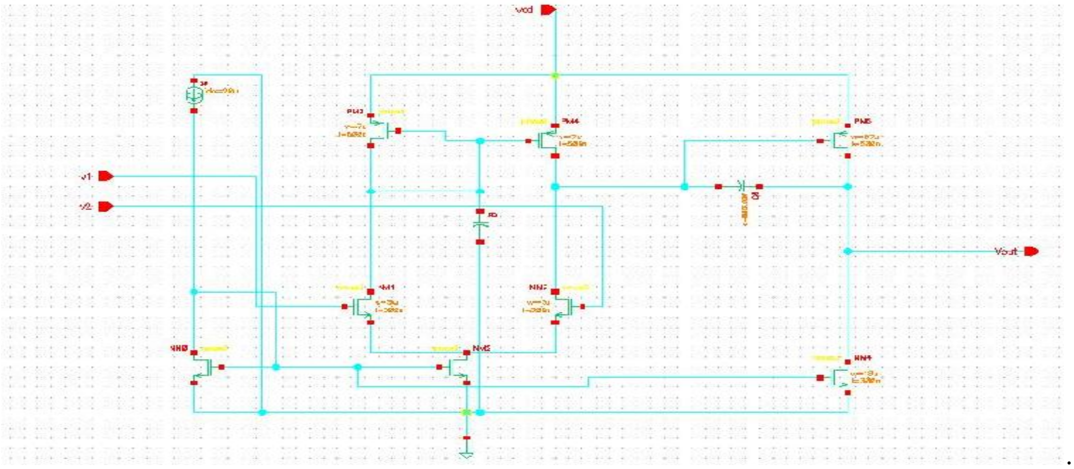

Fig. 5 Schematic of Miller op-amp

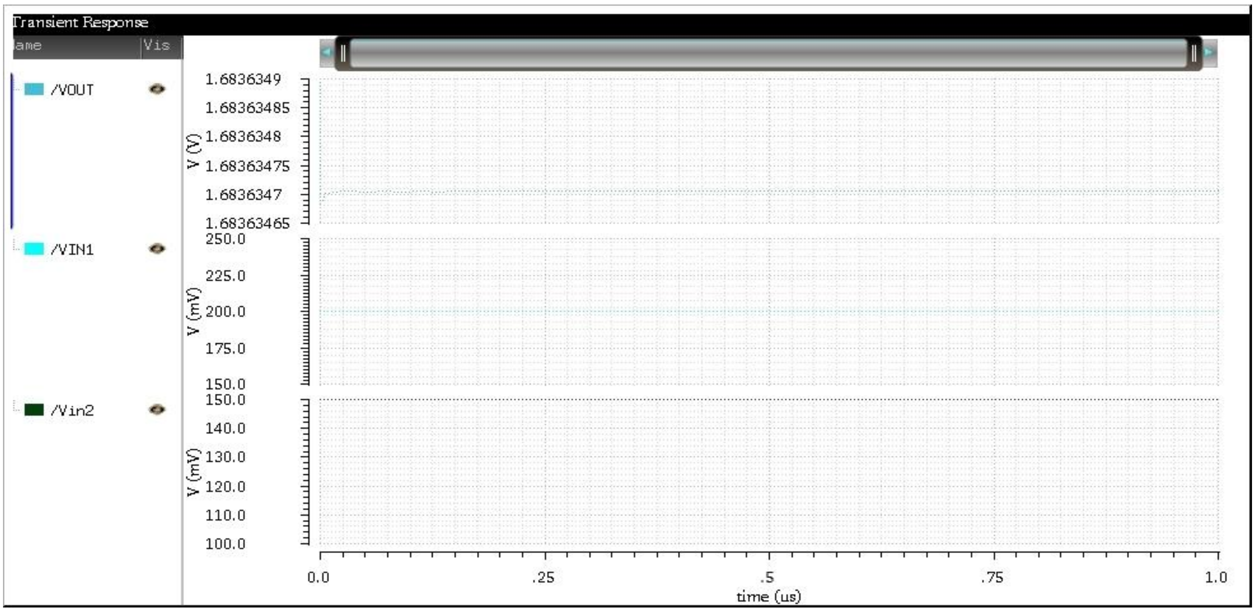

Fig. 6 Output waveform showing Vid

Now calculating the common mode gain ACM

ACM = Vocm/Vcm 3

For Vocm, simulation is performed by keeping Vin1=Vin2 = 200mV.Vocm is shown in Fig. 7

Now Vocm= 3.13µV

Vicm= (Vin1+Vin2)/2= 100mV

Putting values of Vocm and Vicm in Equation 3. Hence value of ACM is

3.13x10-3

Putting values of ACM and AD in equation 6.1

CMRR=33.6/3.13x10-3 =10734.82

CMRR(dB) = 20log(AD/ACM)

=20x(4.0307)

=80.6Db

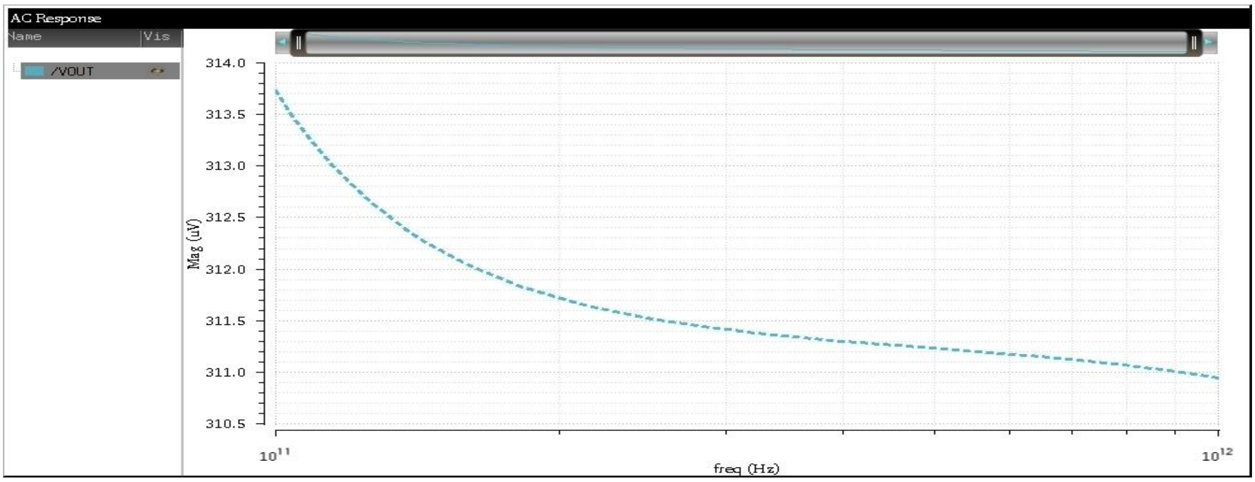

Fig. 7 Output waveform showing Vocm

II MODIFIED PROPOSED INA

Here Rg resistance is replaced with 20pF capacitor to suppress DC offset. R1 and R2 are also replaced with 0.2 pF as shown in Fig. 8. This is done to reduce the offset voltage to a great extent as capacitor blocks DC offset or noise and helps in increasing the CMRR.

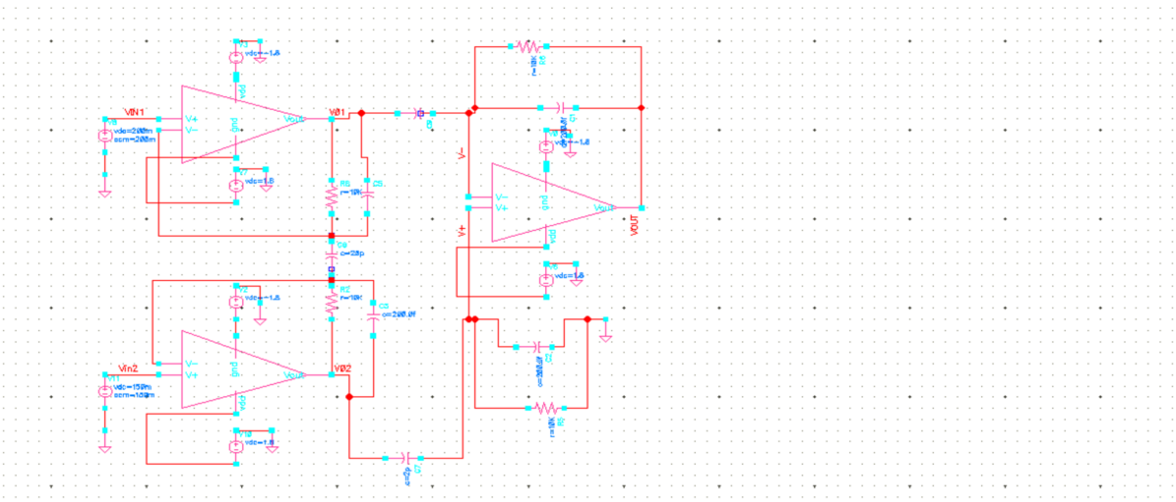

Fig. 8 Schematic of modified INA

The AD of this INA is almost same as that of the INA discussed earlier. ACM is calculated below-

ACM= Vocm/Vicm.Output waveform for Vocm is shown in Fig. 9

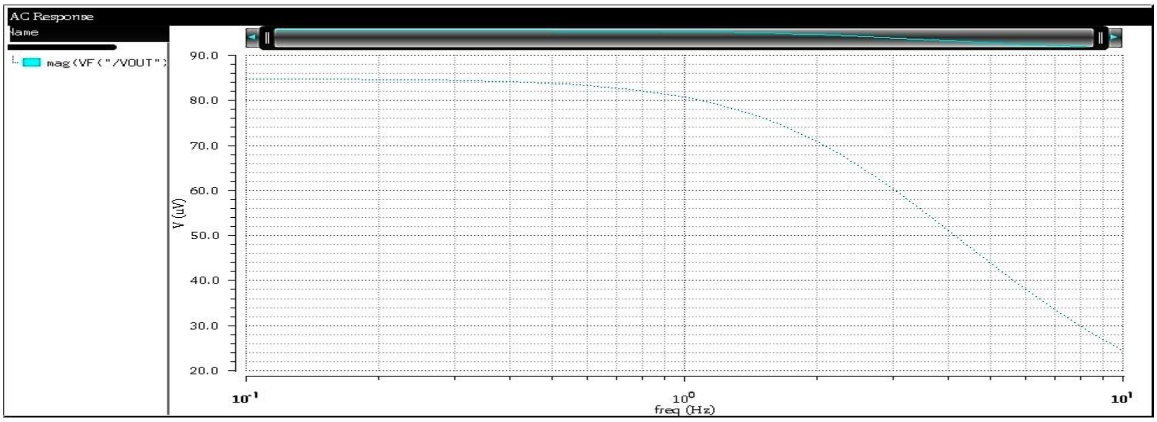

Fig.9 Output waveform of Vocm

Vocm= 85µV

Vicm=100mV

ACM= 0.85x10-3

CMRR= AD/ACM

33.6/0.85x10-3 = 39529.411

CMRR in dB = 20log(AD/ACM)

= 92dB

III. CONCLUSION

INA can be implemented using single stage or two stage op-amps but INA with two-stage op-amps shows better results. Miller op-amp is used as it suppresses DC offset upto great extent.Comparision of the three INAs are shown in Table I

TABLE I
COMPARISION OF DIFFERENT INAS

Parameters	**Conventional INA**	**INA**	**Modified INA**
CMRR(dB)	55	81	92
Power Consumption (milli Watts)	981	641	761.1
Phase margin(degrees)	24	120	124
Gain(dB)	40	55	71

REFERENCES

[1] Azhari, S.J. and Fazlalipoor, H., 2000. A novel current mode instrumentation amplifier (CMIA) topology. IEEE Transactions on Instrumentation and Measurement, Vol. 49(6), pp.1272-1277.

[2] Bakker, A., Thiele, K. and Huijsing, J.H., 2000. A CMOS nested-chopper instrumentation amplifier with 100-nV offset. IEEE Journal of Solid-State Circuits, Vol. 35(12), pp.1877-1883.

[3] Buddhi prakash Sharma, October 2016, "Design of CMOS Instrumentation Amplifier with Improved Gain & CMRR for Low Power Sensor Applications", 2nd International Conference on Next Generation Computing Technologies (NGCT-2016) Dehradun, India 14-16 .

[4] C. Kitchin, L Counts, "A Designer's guide of Instrumentation Amplifier", USA, Analog Devices, Inc (2002).

[5] Crols, J. and Steyaert, M., 1994. Switched-opamp: An approach to realize full CMOS switched-capacitor circuits at very low power supply voltages. IEEE Journal of Solid-State Circuits, 29(8), pp.936-942.

[6] Denison, T., Consoer, K., Santa, W., Avestruz, A.T., Cooley, J. and Kelly, A., 2007. A 2$\mu\hbox {W} $100 nV/rtHz Chopper-Stabilized Instrumentation Amplifier for Chronic Measurement of Neural Field Potentials. IEEE Journal of Solid-State Circuits, Vol. 42(12), pp.2934-2945

[7] Eschauzier, R.G., Kerklaan, L.P. and Huijsing, J.H., 1992. A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure. IEEE Journal of Solid-State Circuits, Vol. 27(12), pp.1709-1717.

[8] Fan, Q., Sebastiano, F., Huijsing, J.H. and Makinwa, K.A., 2011. A 1.8$\mu $ W 60 nV $/\surd $ Hz Capacitively-Coupled Chopper Instrumentation Amplifier in 65 nm CMOS for Wireless Sensor Nodes. IEEE Journal of Solid-State Circuits, Vol. 46(7), pp.1534-1543.

[9] Gray, P.R., Hurst, P., Meyer, R.G. and Lewis, S., 2001. Analysis and design of analog integrated circuits. Wiley.

[10] Kaminska, B., Arabi, K., Bell, I., Goteti, P., Huertas, J.L., Kim, B., Rueda, A. and Soma, M., 1997, November. Analog and mixed-signal benchmark circuits-first release. In Test Conference, 1997. Proceedings., International (pp. 183-190). IEEE.

[11] Khan, A.A., Al-Turaigi, M.A. and Ei-Ela, M.A., 1995. An improved current-mode instrumentation amplifier with bandwidth independent of gain. IEEE Transactions on Instrumentation and measurement, Vol. 44(4), pp.887-891.

[12] Menolfi, C. and Huang, Q., 1999. A fully integrated, untrimmed CMOS instrumentation amplifier with submicrovolt offset. IEEE Journal of Solid-State Circuits, Vol. 34(3), pp.415-420.