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Design and Analysis of 2/3 Prescaler using TSPC DFF at 180nm technology

Jasbir Kaur[1], Mohit Sharma[2]

[1]*VLSI (Electronic and Communication Dept.), Punjab Engineering College, Chandigarh, jasbirkaur70@yahoo.co.in*
[1]*VLSI (Electronic and Communication Dept.), Punjab Engineering College, Chandigarh, mohit8293@gmail.com*

Abstract—A lot of variations are seen in present circuits because of intensive scaling. In this paper 2/3 prescalers is designed and its working operation has been discussed. This work compares conventional 2/3 prescalers circuits and then identifies the circuit on the basis of speed and power taken into consideration. In this paper the total power consumed by this circuit and the maximum operating frequency of 2/3 prescalers circuits are discussed. This modified circuit works at a maximum frequency of 7.41GHz and power consumption is 2.40mW and 2.58mW in divide by 2 and divide by 3 operation respectively. Power supply voltage given is 2V and input signal voltage is 1.2V The entire design has been done in 180 nm technology using cadence tool.

Keywords— TSPC (True Single Phase Clock), DFF(D Flip Flop), Switching Power, Short Circuit Power.

I. INTRODUCTION

- High speed 2/3 Prescaler are the basic elements in a high-speed operation of circuits. This Flip-Flop is the basic element in the frequency dividers used in PLL. Using DFF Dual modulus prescalers in [1] which are required for different division ratio of the high frequency can be made. The main parameters which are needed to be considered in the design of DFF are speed and power optimization.

There are several methods which are used to design DFF with different number of transistors used, it includes CML, TSPC, ETSPC etc. CML is the one which consumes high power and have the highest operating frequency among all. As CML consumes more power so it is not used at low frequencies and can only be used at high frequencies where other circuits cannot work. Among all known circuits TSPC circuit has the lowest power consumption(µW).[2] After reducing one transistor in each branch of TSPC circuit ETSPC is made, but it consumes more power due to short circuit currents which are increased in this circuit.

From few decades It is seen that scaling of the CMOS Technology has been very prominent and the tradeoff between delay and power has become more significant. Therefore, designing a circuit under given specification has become difficult and these two parameters frequency divider are mainly dependent on the D flip flop circuit design.

Considering the above-mentioned requirements, in this design technique of 2/3 Prescaler using TSPC technology has been investigated. Circuits which operates at high frequency, in the order of Gigahertz, fast frequency divider which consumes less power are desired. Analyzing the known topologies for making 2/3 Prescaler, it is observed that TSPC is good in performance if delay and power trade off of the circuit is considered. In this 2/3 Prescaler is being compared with a modified design which uses proposed 2/3 Prescaler circuit which makes this circuit to operate at high frequencies then the conventional 2/3 Prescaler design. These two 2/3 Prescalers are designed on Cadence Spectre tool 180 nm CMOS Technology.

II. CONVENTIONAL 2/3 PRESCALER

In Figure 1 schematic of 2/3 dual modulus prescaler is shown. The maximum operating frequency at which it worked is 5GHz and power consumption is calculated in both circuits, which is 2.58mW and 2.40mW for divide by 3 and divide by 2 operations respectively. Power supply given to this circuit is 2V and input signal is a square pulse of 1.2V and 5GHz frequency. Apparently, power consumption is more in divide by 3 operation as compared to divide by 2 operation.

Figure 6.7 shows the output waveform of divide by 2operation.Here clock signal frequency shows the input frequency which is 5GHz and Qbar signal shows the out frequency which is 2. 5GHz.Power signal is also shown here, which shows the power consumption at different phases of frequency division.

As there is large load [3] on input stage, speed of operation is restricted and large power is dissipated. OR gate and AND Gate introduces extra delay which decreases the speed. Switching power in the conventional design is given by (1)

$$P_{switc\,hing} = \sum_{i=1}^{12} C_{Li} f_{in} V_{dd}^2 \quad (1)$$

Here $P_{switc\,hing}$ is switching power, , f_{in} is input frequency, V_{dd} is supply voltage, C_{Li} is the load capacitance of node s1,s2,s3 and output of DFF1,DFF2 and gates. In figure 4 improved design is shown. These modifications reduce one transistor in second branch of the D flip flops which consequently reduces the number of switching nodes to 8. [4]

Total load capacitance at the second stage of the proposed design is reduced as compared to conventional design. Due to this delay and power of the circuit is reduced. [5]

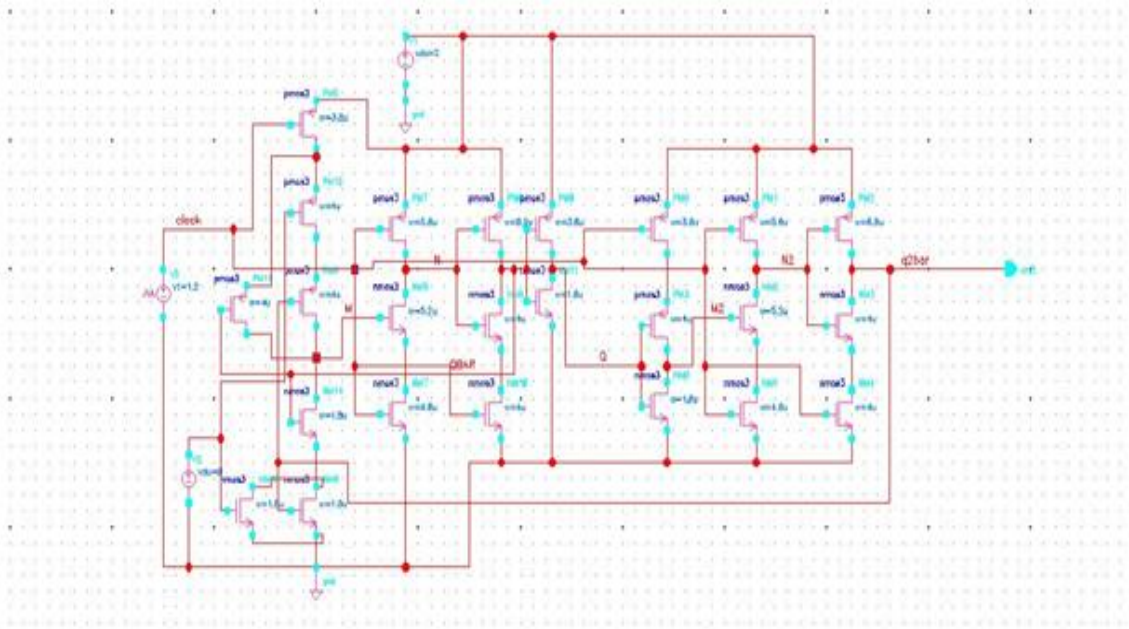

Fig. 1 Schematic of Conventional 2/3 Prescaler

Power saved by reducing one transistor is the power saved which was wasted while switching.[6] Both conventional and proposed design are made using different width for pMOS and for nMOS. Comparing with the conventional design Speed is increased up to 1.482 times.

This design of prescaler increased the maximum operating frequency of circuit in comparison to conventional divide by 2/3 prescaler which worked at 5GHz to 7.41GHz frequency.

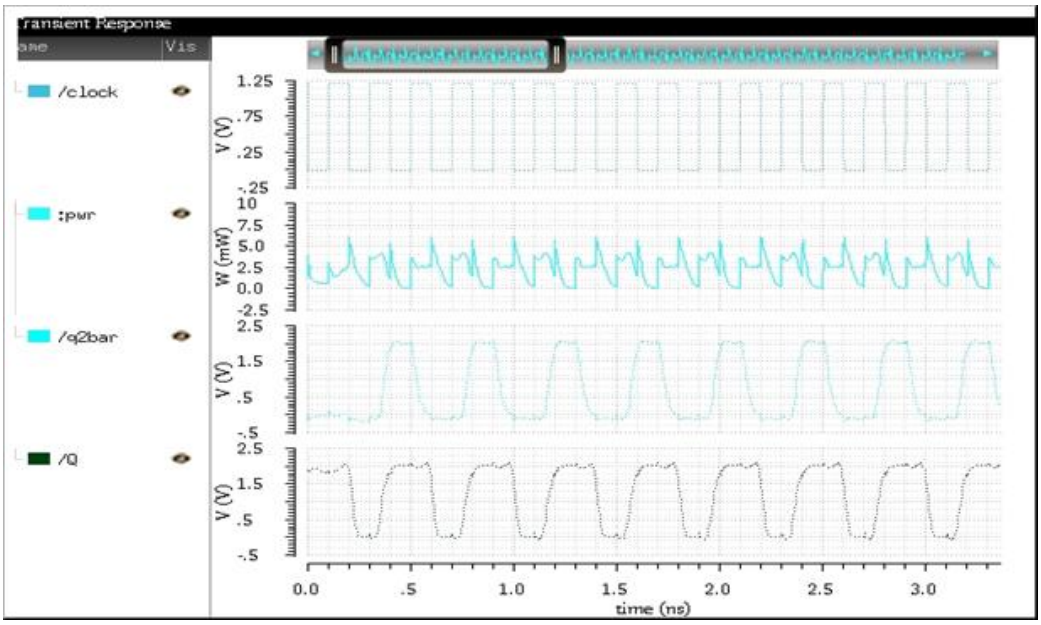

Fig. 2 Waveform of 2/3 prescaler in divide by 2 operation using TSPC DFF

Similarly, Figure 3 shows the waveform of frequency division by 3 which is 1.67GHz.

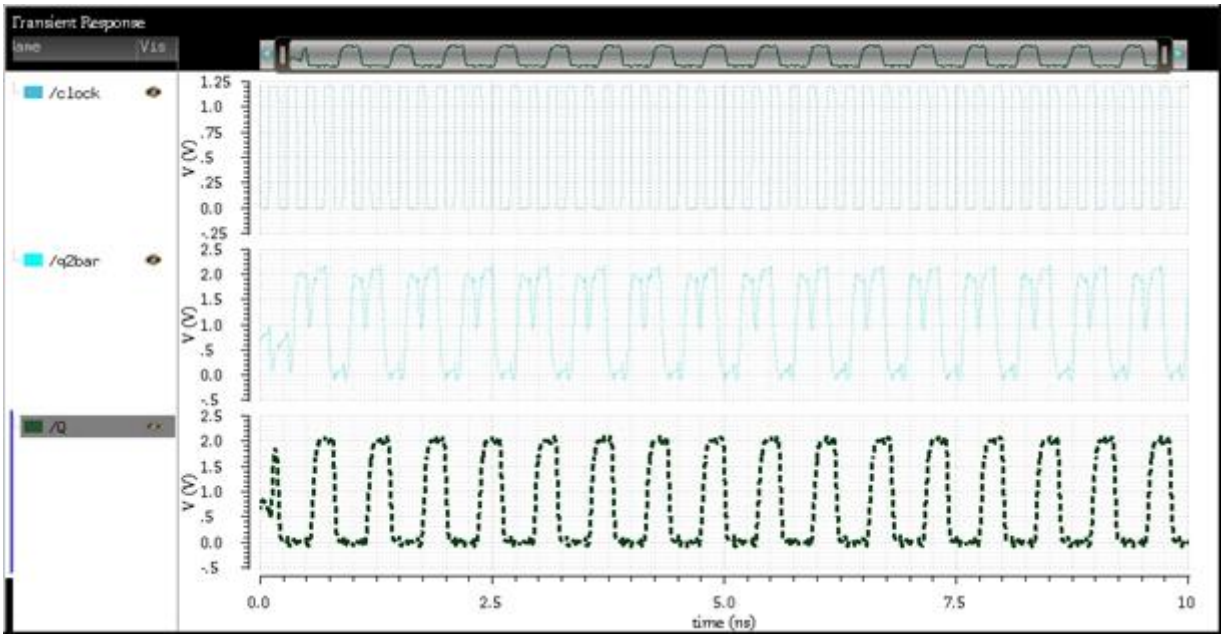

Fig 3 Waveform of 2/3 prescaler in divide by 3 operation using TSPC DFF

III DESIGN OF 2/3 DUAL MODULUS PRESCALER USING PROPOSED TSPC DFF

A. Working at 7.41GHz (Maximum operating frequency)

The maximum operating frequency at which prescaler has been working is 7.41GHz and power consumption is calculated in both circuits, which is 3.65mW and 3.77mW for divide by 3 and divide by 2 operations respectively. Power supply given to this circuit is 2V and input signal is a square pulse of 1.2V and 7.41GHz frequency. In Figure 4 schematic of 2/3 dual modulus prescaler is shown designed using modified TSPC DFF.[7]

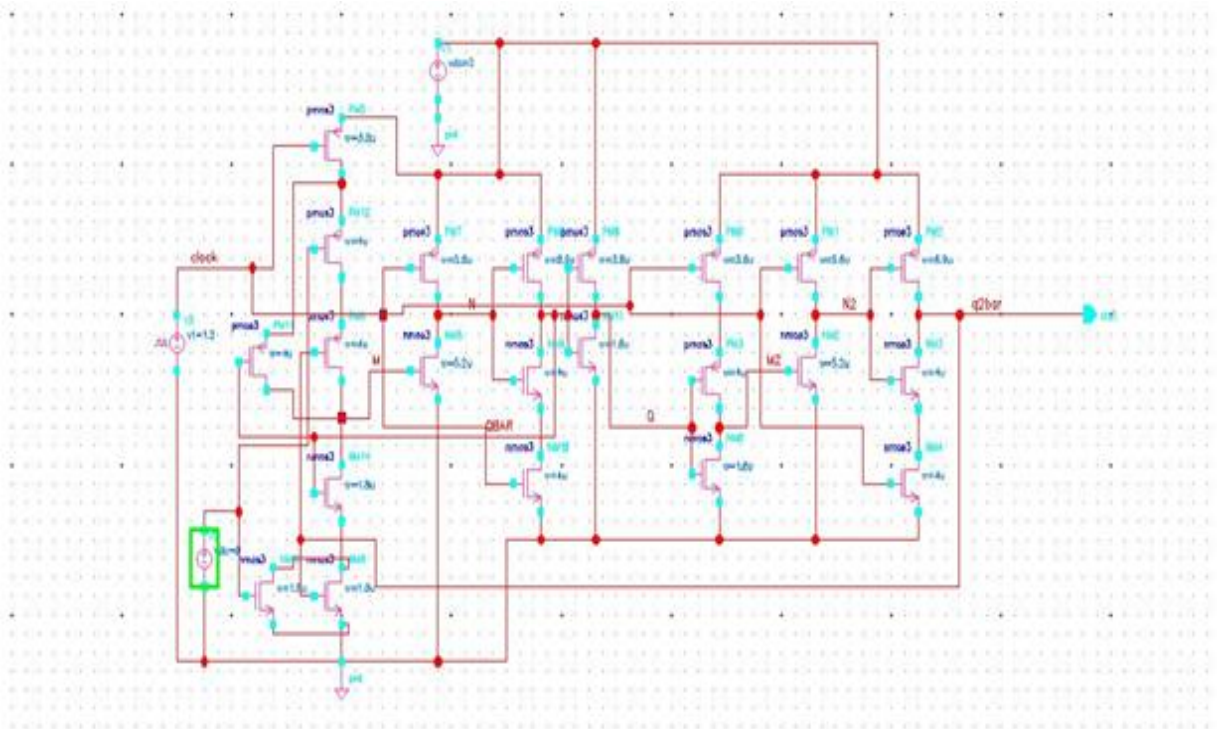

Fig. 4 Schematic of 2/3 prescaler using proposed TSPC DFF

However, power consumption has increased over here which is due to working at high frequency which is caused due to more short circuit power dissipation in second branch of the DFF.

Figure 5 shows the waveform of the divide by 2 operation. Divide by 2 operation works when 1.2 V is given

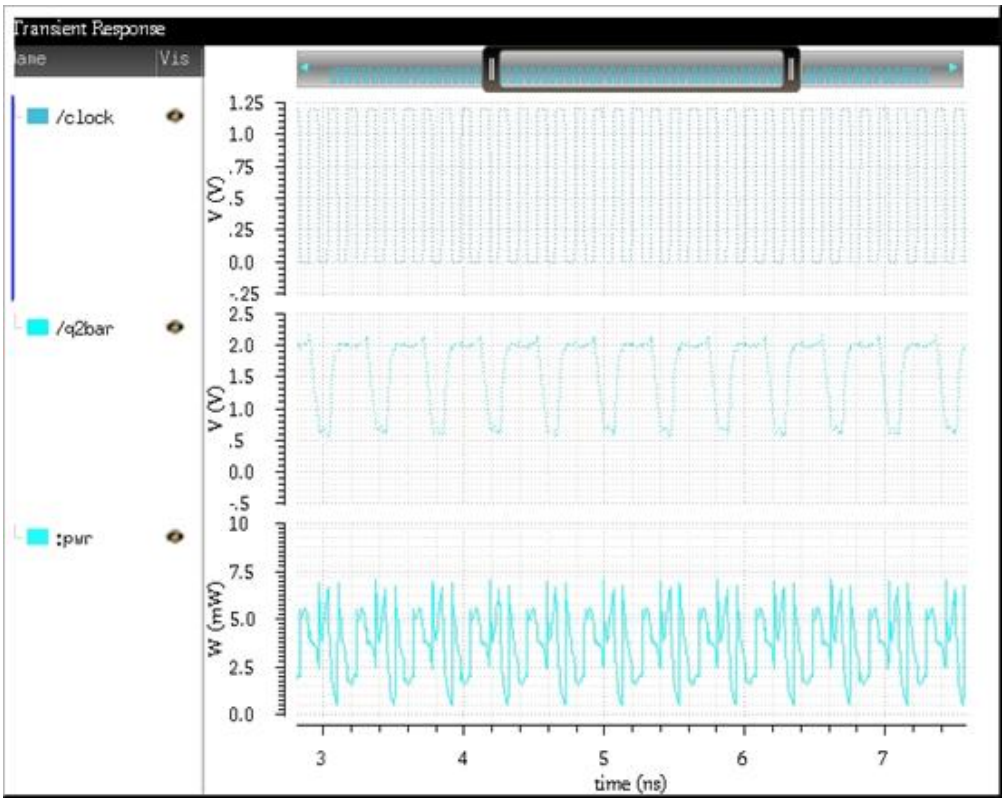

Figure 5.Waveform of divide by 2 operation

Similarly, divide by 3 operation works when 0V is given by the marked supply in the Figure 6.

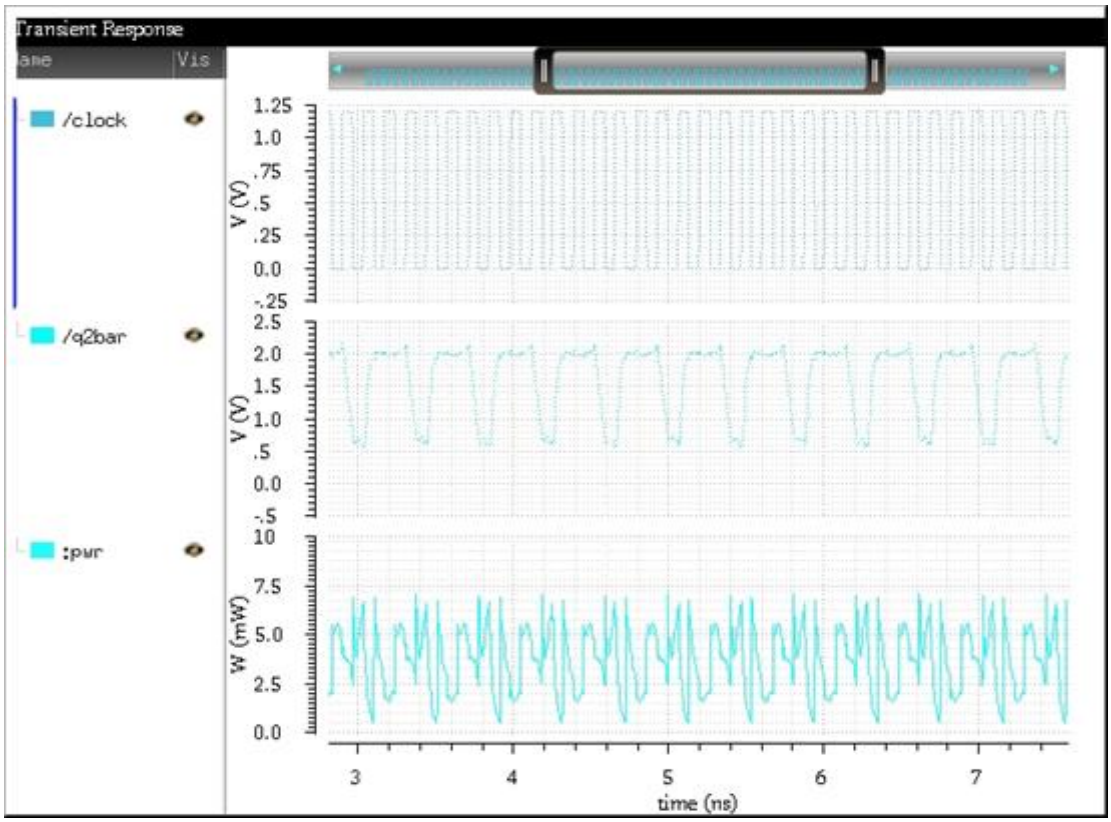

Figure 6 Waveform of divide by 3 operation

IV CONCLUSION

Designing 2/3 prescaler using this modified TSPC DFF it is clear that maximum operating frequency is achieved which is very much greater than the conventional design which works at 5GHz of frequency. The proposed design of 2/3 prescaler also worked at a maximum frequency of 7.41GHz. Moreover, this circuit can work in PLL circuit for making frequency divider as a basic element. In Table I comparison of both circuits are given.

TABLE I
COMPARISON TABLE OF 2/3 PRESCALERS

Design Parameters	**Previous Work Resimulated using conventional TSPC DFF**	**Proposed work using proposed TSPC DFF (Simulated)**
Process(µm CMOS)	0.18	0.18
Supply Voltage(V)	2	2
Max. frequency(GHz)	5	7.41
Power(mW) of 2/3 prescaler at maximum operating frequency	2.40/2.58	3.77/3.65

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