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An Analysis on Various Implemented Scan Insertion Techniques that Reduces the Test Application Time

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Abstract— As VLSI technology is continuously moving to lower technology nodes we need efficient technique for testing [7]. However, reliability and testability will main remain concerned for DFT in today's VLSI design [7]. ATE machines are very expensive. i.e., more number of test patterns will result in more cost. The method of reduction the test application time thereby reducing the number of test patterns will result in reduction of test cost. So, reduction in testing time is must needed because it can makes DFT operation cheaper. In this analysis, we reviewed on an implemented test pattern reordering method by skipping of scan-chain architecture [1] and broadcast based on deterministic pattern generation algorithm [2] is reviewed. Test compression and pattern simulation method, logic cluster controllability and stitching method for reducing the overall test time. In this we are using ATPG tool for generating test patterns.

Key Words— VLSI, ATPG, DFT, Skip-Scan, Broadcast Scan

I. INTRODUCTION

As per scaling ratios are kept improve in on IC's over the years. So, testability of sequential/combinational circuits is became difficult to achieve every time [3]. Because many internal states exists; so, to set sequential circuit can require huge number of inputs due to their internal states [3]. Furthermore, identifying the exact internal state of a sequential circuit from the primary outputs requires higher expertise [3]. Hence, a more structured approach is required as part of a methodical design for testability (DFT) method [3].
The shifting operation and the capturing operation are two main scan operations where care should be taken to guarantee that the scan design can operate properly [3]. The shift operation, which is generally applied to all scan design, must be designed as it operate successfully, in terms of the clock skew that occurred within the same or different clock domains [3]. The capture operation is also common to all scan design, although with many of strict scan design rules in some scan designs as compared to others [3].
It must be designed in a way that the ATPG tool can conclusively augur the expected responses of the generated test patterns [3]. This requires a basic knowledge of the logic simulation and fault models used during ATPG, as well as the clock used during the capture mode [3]. In general, the number of scan chains used is huge, the time to perform test on the circuit is short [3]. So, that the maximum length of the scan chain indicates the overall test application time required to run each test pattern. One disadvantage that for close many scan chains from being used is the presence of high-speed I/O pads.

II. SCAN REORDERING

Scan reordering is used to re-order the scan cells in scan- chains, based on their locations, in a way that it minimize the amount of interconnect wires used to implement the scan chains [3]. During design execution, if the physical location of each scan cell illustrations is not available, only after the final placement process of the physical location of each scan cells illustrations taken into consideration [3].
During the routing process of the physical execution is performed on consideration [3]. During the routing process of the physical implementation, scan reordering is performed using intra scan chain re-ordering, in which scan cells are re-ordered only within the scan chains in which they are belongs to, does not reorder any scan cells which is whole clock or clock-polarity ends and inter scan chain re-ordering, in which scan cells are re-ordered among different scan chains, must make sure that the clock structure of the scan chains is preserved [3]. In these both method, we need to take care about limit the shorter distance between scan cells to avoid timing violation during the shifting operation [3].

III. SKIP-SCAN ARCHITECTURE

After re-configuring of non-violated scan cells in one scan chain. It will take more time to run time for scan_in signal. Because, there is no need to run scan in non-violated cells. That cause the highest no. of scan cells got skipped. i.e., with the assumption of 80-90% of X's were considered as per previous work in [5], [6]. So, we can say that remaining scan chains will have less no. of scan cells. So, those scan chain will take less time for test execution. DFT compiler add TCP in a way that it hold 0 or 1 for entire test session. In this case, we use mux as driving logic [1]. Mux gives 0 by external CI to violation-free scan chain. This way, the whole scan chain can be skipped.

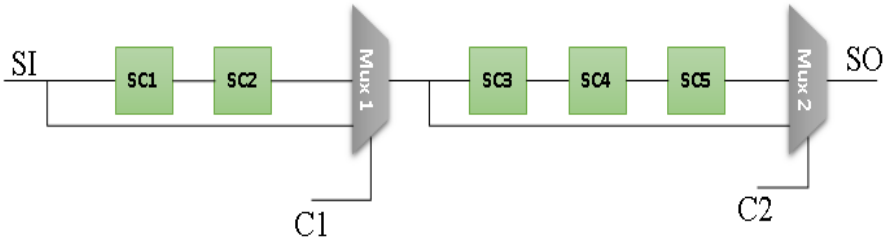

Fig. 1. Example of Skip-Scan design [1]

As per fig.1 [1]. Let for a pattern set consists of 10 patterns, 4 patterns and their past responses have don't care bits in the location of SC1 and SC2 [1]. So, in this method, no shifting of test bits for 8 (4 patterns x 2 skips) test cycles are required, as the path from SI-6 patterns, 5 patterns and their past responses have X's that can be bypassed by taking the path from SC1- SC2-MUX1-MUX2-S0 [1]. The remaining pattern, has don't care bits in all locations, all 6 scan cells can be skirted [1].

IV. CONVENTIONAL SCAN STITCHING METHOD

Stitching of scan cells are performed to stitch all scan cells together to build scan chains [3]. In this method, the response of each scan cell is connect to the scan input of the next scan cell, based on the scan order specified above [3]. In additional, the SI of the scan cell-1 of each scan chain connect to the respective scan chain input port and the scan response of the last scan cell of each scan chain to the respective scan chain response port; so that the scan chains became externally accessible [3].

Suppose, those shared I/O port is used to connect to the scan chain input or response, additional signals must be connected to the shared I/O port to that it always reacts as either input or response, respectively [3]. As discussed earlier, it is must avoid high-speed I/O ports as scan chain inputs or outputs, as the additional loading could result in a degradation of the maximum speed at which the device can be operated [3]. In order to stitching the existing scan cells, lock-up latches/lock-up flip-flops are often applied during the scan stitching for adjacent scan cells where clock skew may generate [3]. So, these lock-up latches or lock-up flip-flops are then stitched between adjacent scan cells [3]. Table 1, shows the experiment results received by Binod Kumar and his team, on Benchmark ISCAS circuits.

V. EXPERIMENT RESULTS

TABLE 1
EXPERIMENTS RESULTS FROM PAPER-1 [1]

Results by Pattern Reordering and Scan Chain Reordering				
Circuits	**Full Scan time**	**Skip-Scan with Scan Chain Reordering**	**Skip Scan with Pattern Reordering**	**Reduction in time (%)**
S15850	61410	55605	31238	43
S38584	178250	159526	64183	60
S38417	548060	471767	84002	82

VI. BROADCAST BASED SCAN COMPRESSION WITH UTILIZING SERIAL LFSR

A. *Linear Feedback Shift Register (LFSR) and Serial LFSR*

LFSR generally used to generate test patterns. Figure 2 shows the generalize LFSR in multiple scan chain. In this, scan chains are connected to the LFSR and LFSR and the test patterns are inserted parallelly to scan chains [2]. LFSR generally behaves like pseudo random pattern generator as it generates the pseudo random patterns [2]. Since LFSR feed patterns in parallelly, the scan chains which are adjacent each other have just 1-bit shifted values, it creates complexity for LFSR to generate deterministic patterns [2].

When in serial LFSR as in figure 2, it is easy to predict which pattern will be generated by solving characteristic polynomials (2^n-1) of the LFSR [2]. Although, since the scan chains having the same value can reduce the fault coverage, it is important to combine similar scan chains and broadcast properly [2].

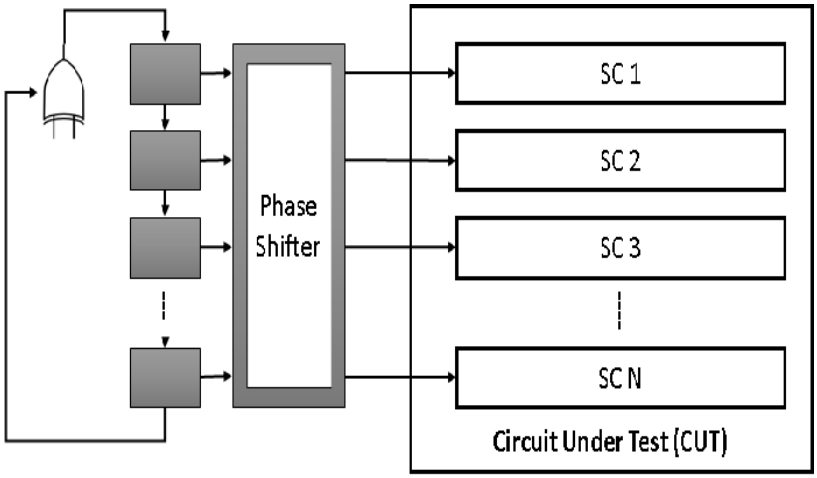

Figure 2: Generalize LFSR in multiple scan chain [2]

Proposed method by H. Lim and his team, utilizes the synthesized LFSR which can generate all deterministic patterns, it is restricted to a single scan chain architecture. For applied into multiple scan chains architecture, multiple LFSR may because one of solutions, however, it increases hardware area overhead besides the volume of test data.

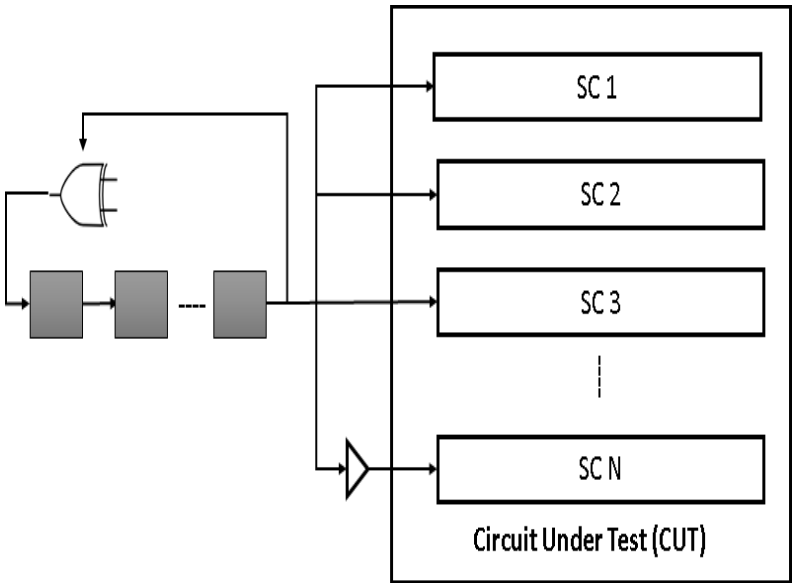

Figure 3: Serial LFSR in scan chains [2]

To solve this, they introduce the concept of broadcast-based scan compression. At first, we'll find compatible scan chains and combine them into a set. In turn, using less number of serial LFSRs synthesized by the algorithm in [4], deterministic patterns broadcasted into the sets of scan chains [4]. The compatible scan set is shown in table 2.

TABLE 2
AN EXAMPLE OF HOW COMPATIBLE SCAN SET DERIVED FROM TWO SCAN CHAINS ? [2]

Sr. No	S.C 1	S.C 2	scan set={1,2}
1	XX1X1X	1XX0XX	Compatible: 1X101X
2	10XX0X	X1XX00	Not: 10XX00
3	XXX10X	1X0X0X	Compatible: 1X010X
4	01XXX0	0XX1XX	Compatible: 01X1X0
5	0XXX1X	XXXX11	Compatible: 0XXX11
6	XX101X	1X1X0X	Not: 1X101X

VII. EXPERIMENT RESULTS

TABLE 3
EXPERIMENT RESULTS FROM PAPER-2 [2]

Circuit	Test Set	#S.C	Compression Ratio (Max. achievable)
S15850	260*611	13	6.37X
S38584	518*1464	12	10.93X
		8	8.93X
S38417	731*1664	32	15.27X
		16	8.95X

VIII. CONCLUSION

By analyzing this paper, we reviewed two different implemented techniques that was designed for reducing the test-time during scan insertion. From the Paper-1, we conclude that we can use skip scan technique can by implementing it with multiple test mode in multiple scan chains insertion methodology which cause we can have DFT debugging more effectively, unless from the both [1] and [2], paper chip area is compromised. Also, we can add any CODEC methodology by which can achieve better compression ratio that also affect on test-time.
For the future work, it will be more effective if it can apply for the advance technology node.

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