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FinFET Based Schmitt trigger Technique

Tejashwini J[1],Sheetal Rao[2],Swastika[3],Swathi PK[4],Dr.Ashwath Rao[5]

[1]*Dept.of ECE, Sahyadri College of Engineering and Management,*
[2]*Dept. of ECE, Sahyadri College of Engineering and Management,*
[3]*Dept. of ECE, Sahyadri College of Engineering and Management,*
[4]*Dept. of ECE, Sahyadri College of Engineering and Management,*
[5]*Dept. of ECE, Sahyadri College of Engineering and Management,*

Abstract— Most of the devices that are used today are portable and it is highly necessary for these devices to have long battery life. The battery life of these gadgets is dependent on the power consumption of the components in the devices. For the good performance of systems, minimization of the power is essential. There are different techniques used to efficiently reduce the power consumption. Different parameters have been calculated and compared. Hence, in order to reduce the power consumption we have designed Schmitt Trigger circuit using one of the leakage reduction techniques called the Dual Sleep Technique. The average leakage power which we obtained in the Dual Sleep method is 9.22699nW, which was comparatively less as that of conventional CMOS. The simulation of the circuit is done using the Cadence Virtuoso Tool.

Keywords— Schmitt Trigger, FinFET, Dual Sleep Technique

I. INTRODUCTION

The VLSI style system has magnified the potency of our technological equipments by amending the assorted parameters like reduction in power offer voltage by applying Method of scaling in fabrication process of CMOS style. Schmitt Trigger is an op-amp which works when positive feedback is given to the non inverting input of the op-amp or differential amplifier. It is a circuit which converts any analog input signal to digital output signal. In this configuration, when the input given is higher than the threshold value, the output obtained is low. When the input given is lower than that of the threshold value, the output obtained is high and when the input value is between the upper threshold value and lower threshold value, the output is retained. Because of this threshold action, the Schmitt Trigger can be used as the bi-stable multi vibrator. Schmitt Trigger is typically used in manipulating the input analog signal to remove noise from digital circuits.

Schmitt Trigger circuits using FinFET technology is used in reducing the leakage power at different supply voltages. A Fin Field-Effect Transistor (FinFET) is basically a MOSFET where the gate will be placed on two or three sides of the channel which forms a double gate like structure which is built on a substrate. Since the source or drain region forms fin like structure on the silicon surface, hence the name FinFET. During the off state, since the channel has been extended there is very less current leakage through the body. This technology also allows the use of lower threshold voltages which results in the better performance and low power dissipation. This also helps us to overcome some short channel effects and also provides electrical control over the conduction in the channel. These FinFETs are able to operate at lower voltages.

In this paper, we analyze the various Schmitt Trigger architectures, 6T, FinFET based Schmitt Trigger, and FinFET based Schmitt Trigger using Dual sleep technique. The circuits are analyzed. The circuits are also compared with each other to understand the differences in them and to know
which architecture is more efficient.

II. RELATED WORK

Now a day's leakage power is the foremost factor to overcome this problem authors have used novel finFET technology. Leakage power measuring obtained using finFET is 12.08pw. Simulation is done with supply voltage of 0.7V and with frequency of 100 MHz. In the paper [2] they have designed FinFET technology with MTCMOS technique. They have also introduced dual sleep technique which is used in reducing leakage power. In the paper [3] the authors have designed FinFET technology with MTCMOS technique. They have also introduced dual sleep technique which is used in reducing leakage power. According to authors better performance in speed, power dissipation, size, reliability, and hysteresis could be achieved by using CMOS device .comparative study of AVLG, AVLS and AVL technique is presented in this paper .circuit was implemented in 45nm technology. They have calculated 21.9% reduction in static power and 16.9% reduction in dynamic power which have also improved overall efficiency. Since static and dynamic power consumption has become the dominant factor, to overcome this, authors have used ultra-low power applications [4]. To overcome this factor they have used controlled-gate FinFET SRAM cells for sub threshold operation and they have compared it with conventional 6T. Authors have presented low-power design technique which plays a major role in reducing leakage

power in Nano scale CMOS by generating the adaptive optimal reverse body-bias voltage [5]. They have concluded that proposed techniques have reduced the leakage power.
In the paper [6] authors have worked with the large combinational circuit blocks and latch-to-latch data paths and they have found out that the novel power gating plays a major role in improving the power-performance trade-off. They have presented multiple sleep mode power gating technique where each mode represents different point in the wake up intern saving the design space .since they have used different mode it allows the processor to save more power resulting in enhanced leakage savings. In the paper [7], they have worked with 32nm bulk CMOS, by keeping sub threshold as a major concern .they have concluded that double gate silicon insulator gives the better performance in the robustness and they are also having better tolerance to variations compared to CMOS.

III. METHODOLOGY

A. 6T CONVENTIONAL CMOS SCHMITT TRIGGER

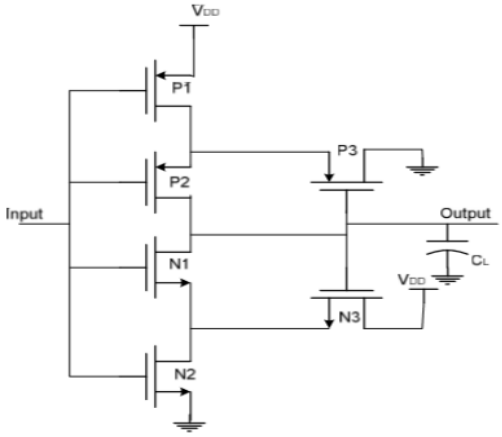

Fig. 1:Conventional 6T Schmitt Trigger.

CMOS Schmitt trigger plays an important role in the electronic system, which can be used in the analog circuit in order to convert a time varying signal to a perfect shape wave like a square wave which would help in solving the noise problem. This circuit is designed in such a way that it can operate the load with faster switching rate, low power dissipation, and at lower supply voltages. It consists of two states like the other multi-vibrators. The circuit's output state depends on the input given, and this will change when the voltage given to the circuit input crosses some threshold voltage which is predefined.
When the input voltage is at 0V and high output state, and when the input voltage gets increased from 0V to $V_{dd,}$ output will be pulled down which is called as the upper threshold voltage. When the input decreases from V_{dd} to 0V then the circuit's output will be pulled up which is the lower switching threshold voltage. The hysteresis voltage can be defined as the difference between the upper switching threshold voltage and the lower switching threshold voltage. The hysteresis of the CMOS Schmitt trigger provides a superior noise margin than the inverter circuit. The Fig.1 shows the basic circuit diagram of a conventional Schmitt trigger circuit. The circuit consists of three NMOS transistors (N1, N2, N3) and three PMOS transistors (P1,P2, P3).

The input given to this circuit can be either a sine wave or a triangular wave. When the input given to the circuit goes low P1 and P2 will be turned ON enabling the output to go high,in turn results in the turning ON of N3. Since the transistor N3 will be in the saturation mode the output will remain as the constant high pulse until the next transition state. When there is transition of input pulse from low to High then the transistor N1 and N2 will gets ON the resulting output will be Low, this in turn turns ON the transistor P3. The circuit is designed in 180nm technology in Cadence tool.

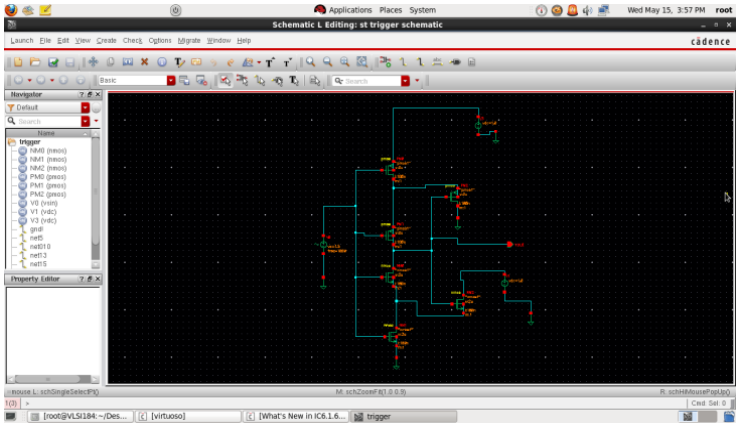

Fig. 2: The schematic diagram of the conventional 6T Schmitt Trigger.

The Fig.2 shows the schematic of CMOS Schmitt trigger circuit implemented in cadence. The supply for this circuit is the Vsine and the source terminal of the PMOS is connected to the Vdd and the source terminal of the ground is connected to the gnd. The Vdd is given as 1.8V.

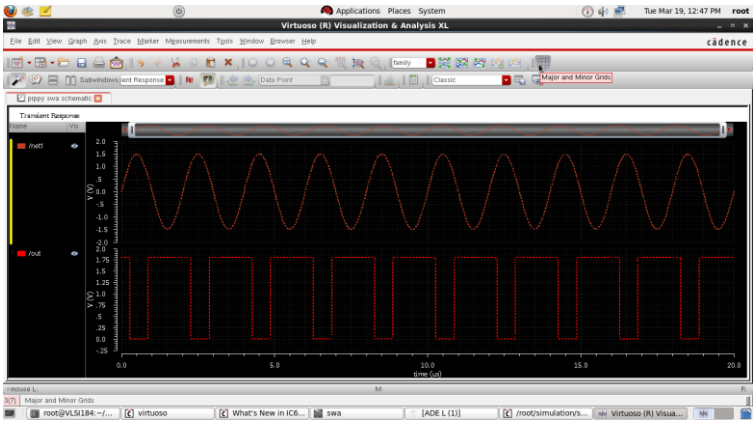

Fig. 3: Transient Response.

From the Fig.3 it is evident that when the input is low the output will be high which means when the input is 0 the output obtained will be 1. Its working is similar to the inverter circuit. And the parameters such as power consumption and noise were calculated.

B. SCHMITT TRIGGER USING FINFET TECHNOLOGY

FinFET device technology is a most promising substitute for CMOS technology because of its better controlling of gate. Schmitt Trigger circuits using FinFET technology as shown in Fig.5 is used in reducing the leakage power at different supply voltages. FinFET design was developed by the University of California, which can overcome the different types of short channel effects.

FinFETs are the 3D structures which raises above the substrate to resemble as fin as shown in the Fig.4. These fins form the drain and the source which provides more volume than a planar transistor. Here the gate wraps around the fin, which provides the better controlling of the channel and allows a very little current to leak through the body when the devices are in the OFF state. This property enables the use of lower threshold voltages resulting in the better performance and the power.

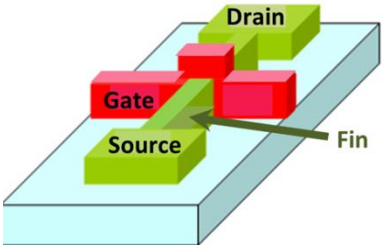

Fig. 4: A Double gate FinFET Device.

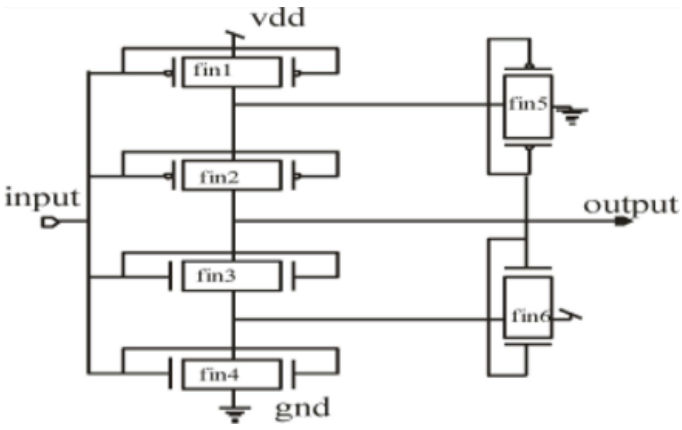

Fig. 5: Schmitt Trigger using FinFET.

The channel in the FinFET is placed above the body and the gate will be attached to it from all three sides, in order to get a controlled and good output from it. So using these FinFETs one can control the voltage in a better way. All the gates of the FinFETs are joined together to achieve a better operation.

The Fig.6 shows the schematic which was implemented at 180nm with a Vsine pulse of amplitude 1 V and the frequency 100MHz and also Vdd was given as 1.8V. This circuit mainly helps us to reduce the noise by shaping the input pulses within the lower threshold voltage and the upper threshold voltage. The resolution of the output was better than the conventional CMOS Schmitt trigger design. The working of this circuit goes same as that of the CMOS Schmitt trigger but with little faster operating speed.

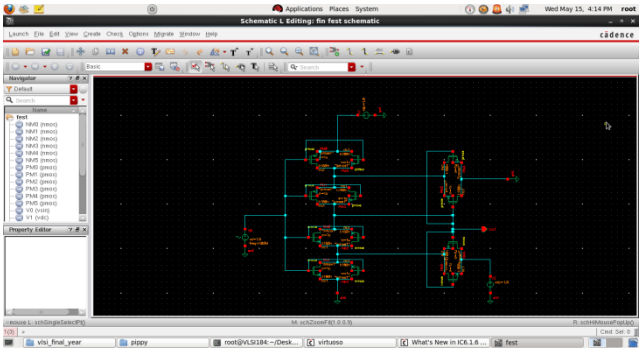

Fig. 6: Schematic of Schmitt Trigger using FinFET.

The Fig.7 shows the transient response of FinFET Schmitt Trigger circuit.

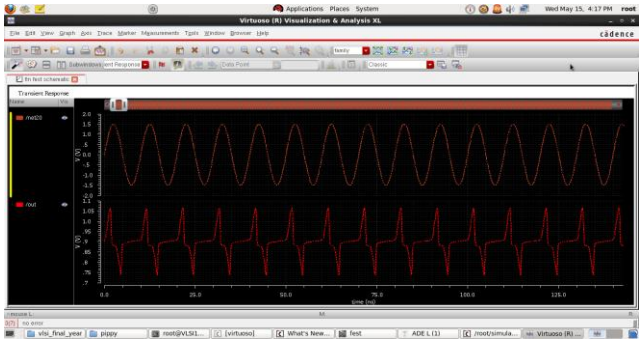

Fig. 7: Transient Response.

C. FINFET BASED SCHMITT TRIGGER USING DUAL SLEEP TECHNIQUE

In this Schmitt trigger design Sleep transistors having higher threshold voltages have been used. A PMOS Sleep transistor is placed between the supply voltage Vdd and the pull-up network and also a NMOS Sleep transistor between the Gnd and the pull down network. These sleep transistors can be turned ON when the circuit is in active state and can be turned OFF when the circuit is inactive. Using this technique we can reduce the sub threshold leakage current by cutting disconnecting the logic circuitry from the supply voltage and Ground in the sleep state. The sleep signal drives these sleep transistors.

The Dual sleep technique uses two extra pull-up and pull- down transistors in the sleep mode either in ON/OFF state as shown in the Fig.8.

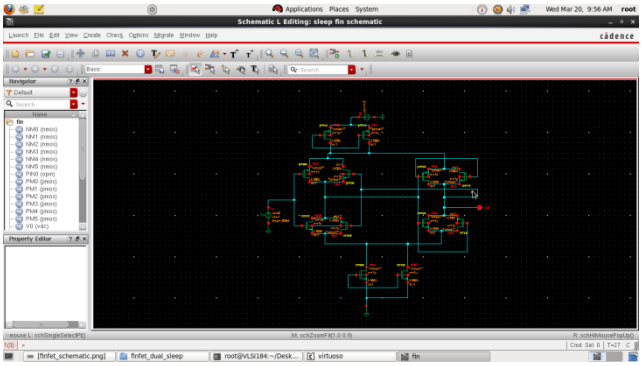

Fig. 8: Schematic of Schmitt Trigger using Dual sleep technique.

Power calculation was done which showed that less power was consumed by this circuit compared to the other two circuit designs of the Schmitt Trigger. The Fig.9 shows the transient response of the Schmitt trigger using Dual sleep technique.

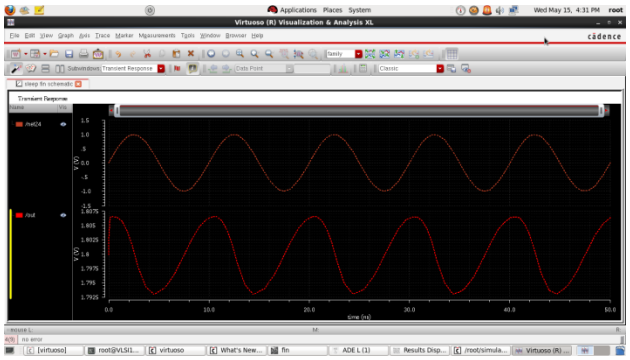

Fig. 9: Transient Response.

IV. RESULTS

Parameters	Power Consumption	Noise
Conventional Schmitt Trigger	59.829µW	$2.73278*10^{-17}$
Finfet	143.185mW	$6.17424*10^{-17}$
Finfet Using Dual Sleep	9.226999nW	$1.32619*10^{-11}$

Table 1: Results obtained.

Here the Schmitt Trigger is implemented using FinFET technology using Dual Sleep technique. From the simulation results, the circuit has a better low power and comparable noise immunity with respect to the conventional Schmitt trigger circuit as shown in the table.1. The simulations were done in 180nm technology using Cadence tool.

V. CONCLUSION

In this paper the Schmitt trigger circuit is designed using Six CMOS transistors, FinFET technology and FinFET based Dual Sleep Technology. The simulation of the proposed circuit is done with supply voltage of 1.8v and with the input frequency of 100Mhz. finally, we conclude that the FinFET based Dual Sleep Technique improves the circuit performance in terms of power and noise.

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