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Fault isolation approach for Test time reduction in DFT at lower geometries

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Abstract— Design for Testability (DFT) is one of the techniques which is used for design become testable after production. This is the review article about testability process now a days the test time reduction and Low pin count at lower geometry are very challenging in industry. For reduce the test time of testability then the simplest way is to increase the pin counts in the chip. Because of that, time get reduced but with time the power and area of the chip get increased simultaneously. Time, area, power are conflicts between each other's so for that challenges, there are so many techniques. This paper describe techniques like, Multi Value Logic (MVL) technic which are combine there concept of adding de-compressor and compressor with the reduce pin count Test (RPCT) this technique is used for solving the noise and error of the decoded test data. The Skip-Scan methodology which is use the Skip-Scan architecture with using Test pattern reordering and Scan chain reordering technique. The Conflict-Reducing Test Point (CRTP) technique is used for reduce the test pattern count of the design by using Test Point Insertion (TPI). It is reduce the conflicts between internal signals a test generation process and ATPG pattern count. By using these techniques industry trying to sort out these problems.

I. INTRODUCTION

Whenever we will increase the complexity of Integrated circuits (ICs), testing them economically becomes a challenging task. Test techniques like full scan enhance controllability and observability of the flip flops in sequential circuits which reduce the efforts in test generation. DFT techniques are required to improve the test generation, quality and reduce the test cost of digital circuit, while at the same time simplifying the test, debug and diagnoses the tasks.

The cost of testability is conflicts with the test pin count, so with the reduced-pin-count test (RPCT) is usually support test compression as well as test speed. It will reduce due to the narrow input bandwidth. For these purpose there is one idea to involve multi-valued logic (MVL) test application with RPCT technology .It will increase the data rate of test channels and also avoid the compromising test speed for the interface.

Test pattern reordering technique is used to maximize test time. For reducing the test time, pattern classification method is classifies the test patterns into different groups with varying skip-depth. This approach known as Skip-Scan which is skipping flip-flops during scan-in.

There is other technique for reduce test pattern count is Conflict-Reducing Test Point (CRTP). It has ability to identify and less conflicts between signals which assign to design internal lines when ATPG is running.

Automatic test pattern generation (ATPG) and the pattern generator EDA tool both are capable for producing tests that offer high coverage of failures occurring in large and complex design. Now, the gate level abstraction and traditional faults like stuck-at fault and transition faults are no longer sufficient to compute at high quality and low-DPM metrics for complex circuits. The new generation tools are targeting time-related and actual-layout-related fault models as n-detect, embedded-multi-detect or cell-aware.

II. FAULT MODELS AND PATTERNS

A. N-detect faults models

N-detect faults model used for achieving higher quality stuck-at tests. It increases the probability of fortuitous detection of defects that do not behave as stuck-at faults. Its test size tends to grow linearly with n. It prevents the use of n-detect tests when it becomes impossible to fit such a large test on a tester with limited available vector memory or test application time.

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B. Multi-detect faults models

Embedded multi-detect ATPG algorithm embeds additional detection of already detected faults (Like stuck at faults, transition level faults, bridge-faults) in regular single-detect ATPG patterns. Embedded Multi-Detect ATPG exploits don't care bits to detect faults multiple times. It is used to generate test patterns for all our industrial designs. ATPG requires more compute time to embed extra fault detections in each pattern compared to conventional 1-detect stuck-at ATPG. In this way, we can increase the test quality in a similar way as n-detect tests, without increasing in test set size.

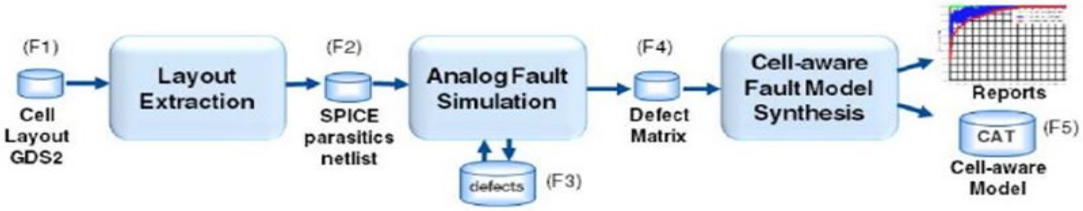

Fig.1 Test Library

C. Cell-aware test pattern

Cell-aware test fault model is based on post-layout transistor-level net-list which include defect-based ATPG approach. CAT is detecting cell-internal defects and demonstrated through high-volume production test results. CAT achieved the low defective-parts-per-million (DPPM) rates. It has two major parts.

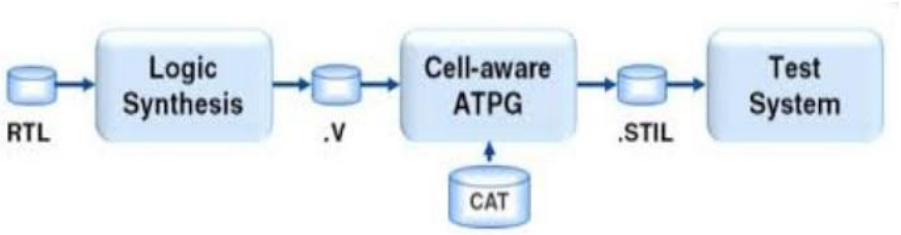

Fig. 2. Well-known design flow.

Technology-dependent CAT view generation flow is first part, which is one-time task and for development of CAT methodology, layout extraction is followed by fault simulation and fault model synthesis to create the CAT library models. Fig. 1 is show the Cell-aware test library view generation.

The second major part of this methodology, is well-known design flow. Fig. 2 is show the CAT well-known design flow. In this CAT ATPG is used instead of traditional ATPG. CAT ATPG generate patterns for very large multimillion gate designs. These methodology increase the defect coverage and reduce the defect rate which is measured in DPPM.

III. FAULT ISOLATION APPROACHES

A. Multi-valued Logic (MVL)

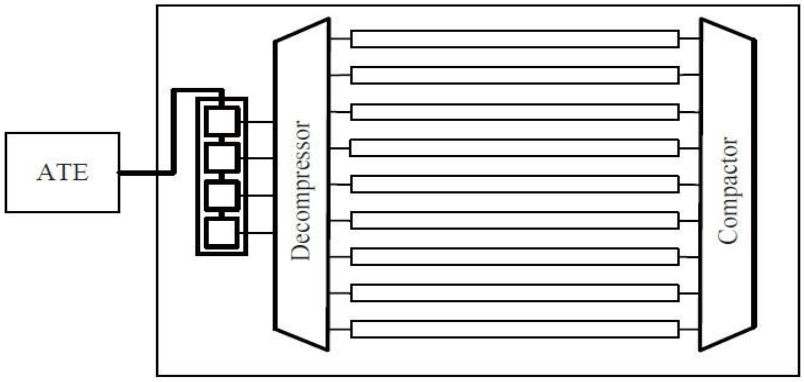

Fig. 3.RPCT with decompression interface.

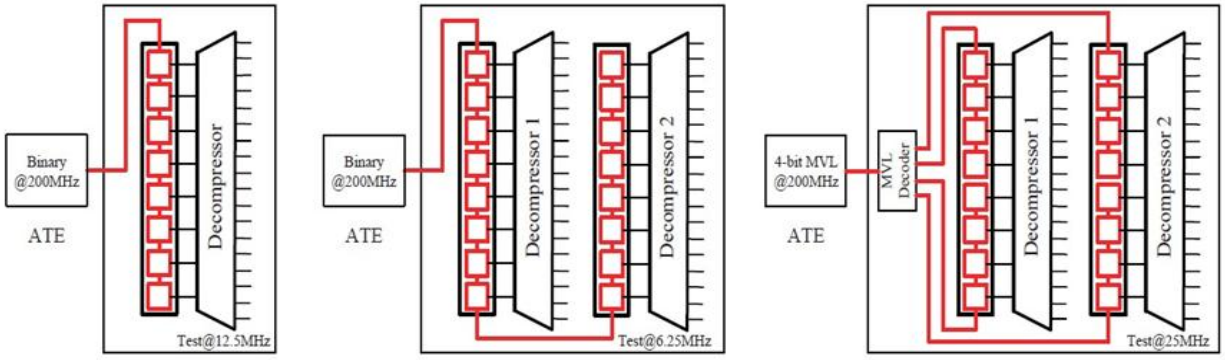

Fig. 4. Test speed improvement by MVL signal transmission

For reduce the cost and number of pin count in DUT the Reduced Pin Count Test (RPCT) technology used. Which is shown in Fig. 3 of RPCT with decompression interface model. Which sends serialized data through less number of test channels and de-serialized them in DUT. It is done by creating some modification in Test Access Mechanism (TAM). There is bandwidth mismatch between fast ATE channel and slow DUT scan speed. So, for solving these claim we can use MVL technique. It increases the data rate of test channels and enhances the data transfer capability in RPCT, we can change the data format of test channels to MVL.

When RPCT interface with MVL test channels, we can assume that ATE channel is capable of generating 200MHz signal. When neither RPCT nor test compression is used, a 200MHz test channel can support 200MHz scan speed for a single scan chain design. In Fig. 4 there are different test speed improvement models used by MVL signal transmission which are improving the speed by increasing in the ATE.

This technique identifies some error sources like data converter nonlinearities and noise. To deal with nonlinearities, a calibration procedure is conducted before applying test data. To solve the Noise and error of the decoded test data a retest scheme is adopted.

MVL does not exist in currently available ATEs, some external modules can be developed for MVL transmission and calibration.

B. Skip-Scan methodology

This technique is maximize the number of skip of scan cells and it is used for steering logic to control the reconfiguration of scan chains so it reduces the test time and test cost. For that propose Skip-Scan architecture is used which is shown in Fig. 5. These methodology stated by dynamically reconfiguring scan chains, some of the scan cells can be by passed while change in/out of test patterns.

The effectiveness of this technique lies on the assumption that more number of don't care bits are present in test patterns and their results. In compacted test cubes, the position of multiplexers are determined based on given test set. These multiplexers are controlled by a controller with finite state machine, scan enable signal, reset signal and combinational logic arrangement.

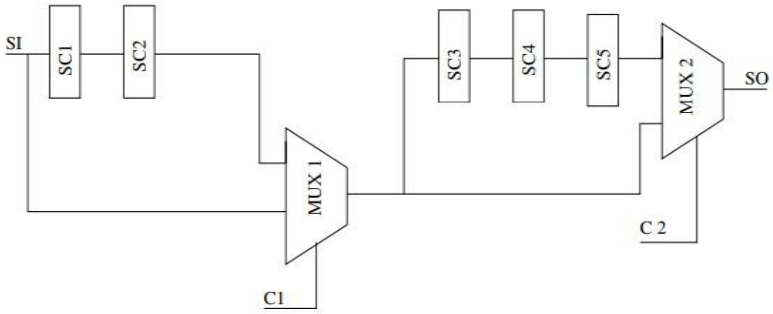

Fig. 5. Skip-Scan Architecture.

In addition, to reduce test application time, the proposed methodology minimize the switching activity as the number of scan shift operations are being reduced. Further, as the scan cells are to be bypassed, we get reduction in test data volume too.

Pattern recording can be applied in conjunction with scan chain reordering to obtain advantages of both methods for achieving further reduction in test time.

C. Conflict-Reducing Test Point (CRTP)

In this new DFT technique, that goals to reduce test pattern counts through an innovative conflict-reducing test point identification methodology. It is used to overcome the growing test set problem, as it significantly reduced the number of test patterns test application times.

Test point insertion (TPI) techniques attempt to improve the fault detection by minimizing hardware at real estate. They select internal lines from the circuit and add control point (CPs) and observation points (OPs) for excite faults. Generally, optimal TPI circuits with re-convergent fan-out is an NP-complete problem and it's identify suitable CP and OP location and improve the circuit testability. For that purpose, in scan chains extra gates and wires are routed or additional flip-flop to be included.

Usage of CRTP, a new class of test points that can be deployed to first reduce conflicts between internal signals a test generation process is handling and reduce ATPG pattern counts.

The conflicts between internal signals manifest themselves in a different-different ways, there are two fundamental types of conflicts that can be found in digital circuits when ATPG is running. These conflicts are describe in [2].

This method is designing digital circuits for low patterns counts by removing conflicts between internal signals that prevent merging of test cubes for multiple faults. The method works in test compression environment and enhances it by 3-4x.It is expected to extend the life of test compressor for another 2-3 technologies nodes.

IV. CONCLUSIONS

This review paper describe about different-different techniques for the Design for Test challenges. Through these techniques we can reduced the parameters such as power, area, time and cost which all are conflicting with each other inside testing techniques. According to our observation from this paper explaining three techniques which are Multi Value Logic (MVL), Skip-Scan Methodology and Conflict Reduction Test Point from these techniques the Conflict Reducing Test Point is the effective technique for testing because it reduced number of test patterns and application time compare to others two techniques.

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