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Smart Embedded Audio & Video System based on Zynq-SOC

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***Abstract:** This paper presents a unique design of software and hardware co-design for audio and video processing system. Video and audio surveillance is the major application of this work. The peripherals required for the implementation are a zynq board, an ov7670 camera module and an electret microphone. Xilinx Vivado 2018.1 and SDK 2018.1 were used to design and implement the hardware and software respectively. To display the output of camera module, a VGA monitor is interfaced with zynq soc and the audio heard by the microphone is fed to the speaker connected to the Zedboard line out/ head phone out. The application is developed using C language. By analyzing the device utilization summary, it is clear that, this system is consuming less power and low design area, designing time and will be used in real-time with good results.*

Keyword--- ADAU1761 codec, Electret microphone, embedded audio & video system, ov7670 camera module, Zynq 7020-SOC.

I. INTRODUCTION

Optimizing a design gives good results that include performance of the system, power consumption of the circuit and the area required for the design when compared to the non-optimized design. The delay of a system can be reduced by reducing the design area by shortening the length of interconnects. One of the better ways to reduce the design area is using latest technology, means usage of small components in terms of nanometer technology. FPGA's are reconfigurable devices which are having only programmable logic but not having any processing unit. A soft core processor will be implemented on the programmable logic. But, the soft core processor is limited to its operating frequency. Hard core processors are able to achieve high operating frequency when compared to the soft core processors. By using these types of devices, a separate processing system is required to process the logic stored in the programmable logic and it requires a large area. Then the term miniaturization comes in to picture. A device which has a processing system along with the programmable logic gives a solution for the minimization of the design area. As the processing system and programmable logic are integrated on the same chip it is called as system on chip (SOC). As the name embedded audio & video system, it is the combination of hardware and software. Miniaturized PC, OV7670 camera module, Microphone, VGA monitor and speakers will make it possible to design compact embedded audio & video system for a particular application. To design such a system proper computing system is required and it is the only key design metric. Many solutions are provided based on general purpose processors (GPP), Digital signal processors (DSP), Reconfigurable devices (Field Programmable Gate Array) FPGA [1]. ZYNQ-7000 SOC-FPA is used for designing the audio and video system. It is an all programmable SOC to combine both hardware and software in to single device, and provides high performance, flexibility, scalability, low power. Zedboard has Processing System (PS) [2] and Programmable Logic (PL) [3]. Dual-core ARM CORTEX A9 is the Processing system which operates at 1 GHZ. Artix-7 FPGA is the Programmable Logic having reconfigurable resources like 140 BRAMs, 13,300-logic slices, DSP48E1s-220, XADC hard IP block used for hardware functionality. The advanced extensible interface (AXI) is used to interface processing system and programmable logic. AXI belongs to third generation of advanced microcontroller bus architecture and is used for high-speed interconnect.

In order to work with high speed FPGA's an advanced IDE is required. Xilinx introduced Vivado IDE for advanced FPGA's. It is used for creating the hardware bocks with the help of hardware description languages like VHDL and VERILOG. Vivado has a unique feature that, it can able to package the source code in to an IP Core which can be used for later uses. The hardware required for the design will be implemented in the Vivado. To create software application SDK (Software Development Kit) is used. SDK has all the required tools like BSP's (Board Support Packages) for all the Zynq board that are useful to create connection between the software and board. Application software's will be created using C/C++ languages.

II. METHODOLOGY

Required design tools and target hardware platform for audio and video system are, Zedboard as target hardware, Vivado 2018.1 for hardware designing SDK 2018.1 for Application software. Peripheral modules are OV7670 camera module, an electret microphone, 3.5mm audio cable, VGA monitor and speaker/headphones. A bitstream file with an extension (.bit) is created in the Vivado which is a machine readable file in the form of 0s and 1s. This bitstream defines the behaviour of the hardware. By exporting the hardware the tool can create a workspace in the SDK to create application software. This application contains the working of the hardware. Creating application software will automatically generate a board support package for the ease of connecting hardware board to the application software. All the required

drivers for the IP cores defined in the hardware are assigned with proper drivers in order to with the application software. By adding the code, which defines the hardware functionality the application software is configured as per the user requirement. By programming the target hardware with proper bitstream file and running the application software the behaviour of the system will be tested in real time.

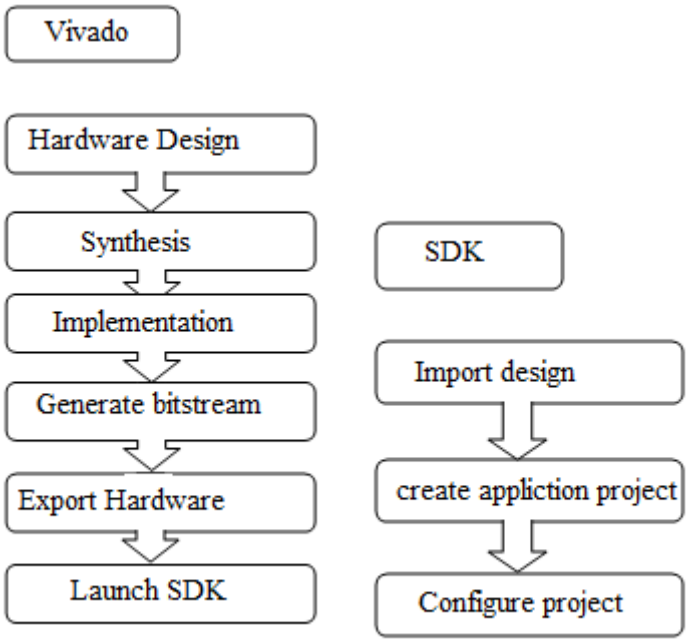


Fig.1. Top level procedure of proposed system.

III. ZYNQ ARCHITECTURE

Zynq-7000 SOC-FPGA is the latest release from the Avnet family. Everything it has is programmable like the Input/Output (I/O) PINS and CLB's etc. Zedboard is a System on chip. It means, the required things like programmable logic, processing system, memory elements are all fabricated on a single chip [6]. as zedboard having both the programmable logic and processing system on a single chip it has a name processor-centric platform. this board is used for different type of smart applications as it is having the advanced features.

The fig2 depicts the architecture of Zynq-7000 SOC. It enables the implementation of design logic in PL and runs application software in PS. The processing system ARM CORTEX-A9 will support the Linux operating system and it can support some other operating systems. It has a hard core processor (ARM cortex-A9) in Processing System (PS) and a soft core processor (MicroBlaze) in programmable Logic (PL). These types of FPGA soft core processors are most useful for reducing the design time.

Separate power domains are provided for the Processing System (PS) and Programmable Logic (PL) in Zedboard. These power domains are independent of each other and will be turned OFF if required. The processing system boots first and then programmable logic if required. The PS comprises of Memory elements, Application Processing Units, I/O pins, and interconnects [7]. A couple of ARM processors, each one having an individual computational units, a NEON media processing engine (MPE), Memory Management Unit (MMU) and Floating point unit (FPU) are inbuilt within the APU. Level 1 and Level 2 cache memories are involved in the Memory Management unit (MMU). For the purpose of storing data and instructions Level 1 has (32kb+32kb) in two sections. Level 2 has (512kb) cache and on-chip memory (256kb). The connection between on chip memories and ARM cores is done by a snoop control unit.

Different operating modes are provided by the processing system (1) a single core is able to process the operation while the second core is in OFF mode. (2) Both cores will be turned on and work as symmetric or asymmetric. If a common operating system is used for dual Cores it comes under symmetric mode. If each core is operated by a dedicated operating system it comes under asymmetric mode. A trust zone technology is offered by the Zynq Processing System for secure mode operation. Dynamic and static memory controllers are existed in the memory interface unit. Multiuse pins of the Zedboard are used for communication between external devices and I/O devices. These pins are used to establish services like GPIO, SPI, UART, TIMER, ETHERNET, and USB. Data transmission between Cortex-A9 and Artix-7 is done by high performance interfaces. AXI ports are used for data transmission between programmable logic and processing system.

Programmable Logic (PL) has Control Logic Block (CLB) which is divided in to two logic slices. Each slice consists of 4 Look-Up-Tables, Flip-flops and other logic. A single LUT may capable to implement logic for up to 6 inputs, small ROM, RAM, a shift register and PL has resources DSP48E1S used for high speed arithmetic and Block RAM (BRAM) used for dense memory requirements.

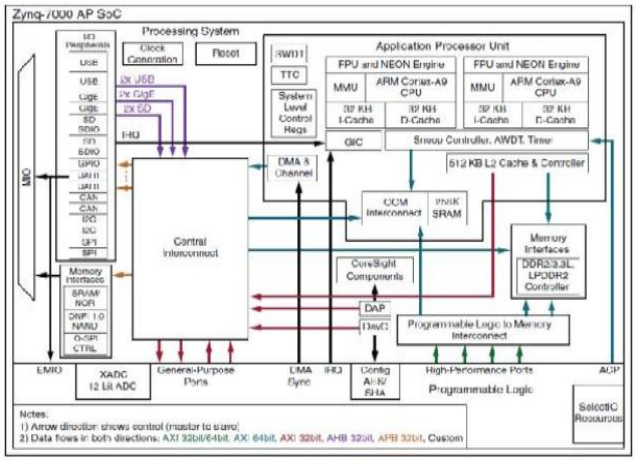


Fig.2.ZYNQ Architecture

IV.ADAU1761 CODEC & OV7670 CAMERA

The embedded audio & video system comprises of hardware and software. The main hardware role is played by the audio codec for audio processing, which encode and decode the audio signals. Vision is processed by the OV7670 camera. The audio codec used for this work is ADAU1761 [8] from Sigma DSP is a low power, stereo with integrated digital audio processing which supports 48khz record and playback at 14 mW from 1.8v analog supply.

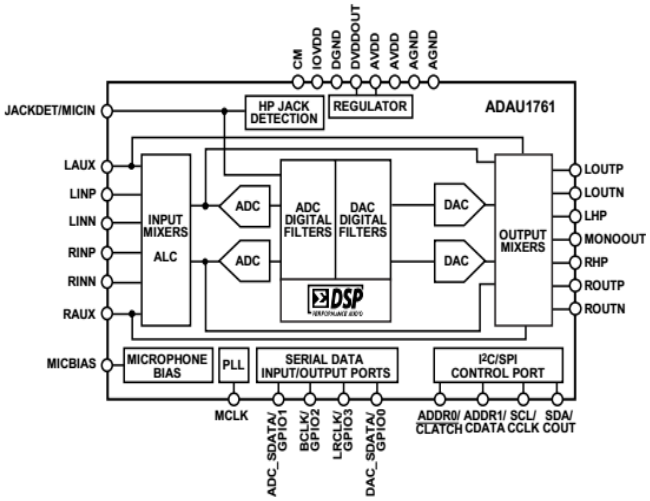


Fig.3.Functional diagram of adau1761 codec

The sample rate supported by the stereo ADCs and DACs is from 8 kHz to 96 kHz and also used it as digital volume control. It has features include 6 analog input pins, flexible analog input/output mixers, PLL supporting input clocks from 8 MHZ to 27 MHZ, Analog automatic level control (ALC), IIC and SPI control interfaces. A functional diagram for ADAU1761 is shown in the figure 3.

The functional description of the ADAU1761 gives the working of the audio codec. Input is applied at input mixers through the input channels LAUX, LINP, LINN, RINP, RINN, and RAUX. An Automatic Level Control (ALC) in integrated within the input mixers. It is used to continuously adjust the gain to keep the recording volume constant as the input recording volume level varies. SERIAL DATA INPUT/OUTPUT PORTS are used to receive/transmit the data in a serial order. It has different clocks like BCLK, LRCLK for providing different clock frequencies for the transmission of the data between hardware. ADAU1761 has two types of control modes and it is operated in one of the two modes. The two control modes are IIC control and SPI control. This codec has an inbuilt regulator with different modes (CM, IOVDD, DGND, DVDDOUT, AVDD and AGND) to provide different voltages as per the requirement of the power supply for ADC, output driver. The applied input signal fed to digital filters through analog to digital converters (ADC). Then the digital signal is again converted to analog by using digital to analog converters (DAC) and fed to output mixer through DACs.

At the output mixers output channels LOUTP, LOUTN, LHP, MONOOUT, RHP, ROUTP and ROUTN are used to connect the output load. MICROPHONE BIAS is a voltage for Electret Microphone. PLL uses the MCLK as a reference to generate the core clock frequency.PLL has different operating modes such as Integer mode and Fractional mode. Pin configuration of the ADAU1761 is shown in the figure 4.

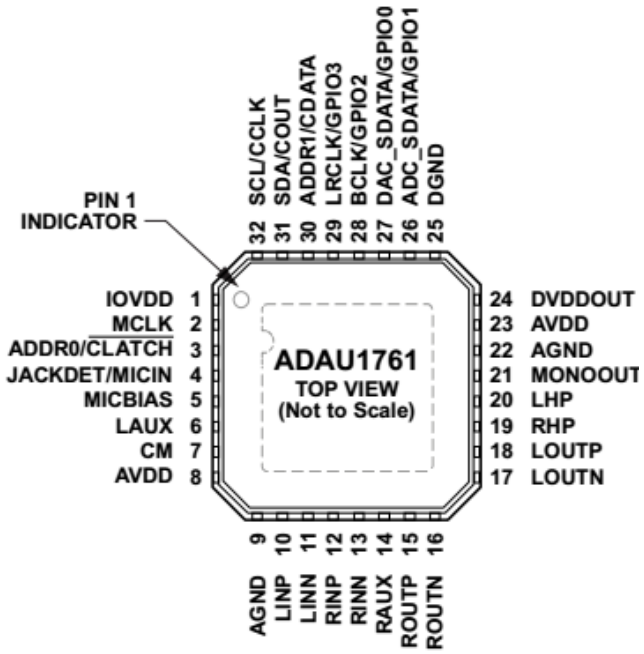


Fig.4.Pin configuration of adau1761 codec

OV7670 Camera:

OV7670 camera module is low power CMOS device. It is an integrated circuit of image processor and VGA camera. Seial camera control bus (SCCB) is used to controll the camera module. It outputs 30fps in VGA with user control on the image quality and resultant data. Different output formats that are produced by the camera are RGB,raw RGB,GRB 4:2:2, RGB 565/555/444, YUV (4:2:2). It operates at a very low voltage of +3.3v for different embedded smart applications. This camera is high-sensitive to low light operation and some of the image quality features include color saturation, hue, gamma, sharpness etc,. working diagram is shown in fig 5

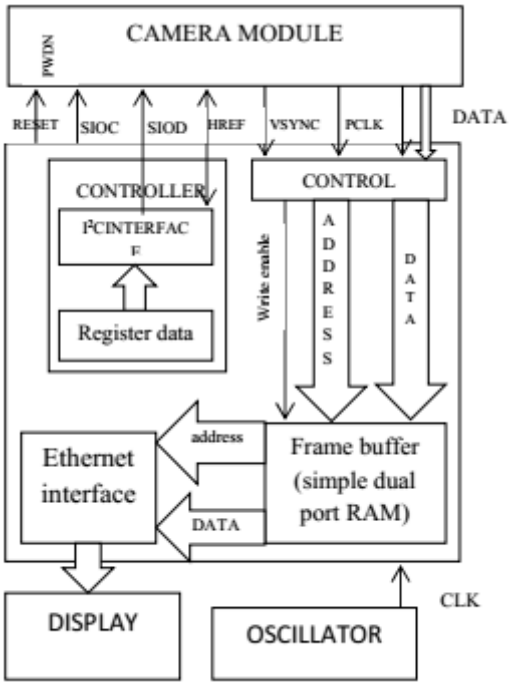


Fig 5. Functionality of OV7670 camera

An oscillator is used to provide clocking source to control the camera module's XCLK pin. Serial communication is done by IIC. By properly configuring the internal registers of the camera module through IIC, the module send pixel clock signal and data outputs (D0-D7) with synchronization of HREF and VSYNC which represents the active pixels and active frame respectively. The camera module is connected through the peripheral module (PMOD) ports of the Zedboard. Fig 5 shows the complete set up of embedded audio and video system.

V. MICROPHONE/LINE IN INTERFACING

Microphone is a transducer which converts audio signals into electrical signals. It is directly plug in to MIC in jack of the Zedboard. A line in cable is used in this work to feed input from an audio device. A 3.5mm audio cable is connected to LINE IN jack of the Zedboard and other side is connected to the audio output jack of an audio device.



Fig.5. Electret microphone

VI. IMPLEMENTATION OF DESIGN

To implement this work, Xilinx Vivado 2018.1, and Xilinx SDK 2018.1 tools are used. The hardware used is Zedboard, a low voltage CMOS OV7670 camera module, VGA monitor, and an electret microphone. Block design was created in the Vivado 2018.1 and IP modules Zed_audio_ctrl, NCO (Numerically Controlled Oscillator), Camera IP, VGA IP, Clocking IP, Debounce IP, Block RAM and AXI GPIO are created and packaged using Vivado IP packager. These IP's are combined in AXI-4lite to interface with processing system of the Zedboard. The implemented design is illustrated in the following figure 6.

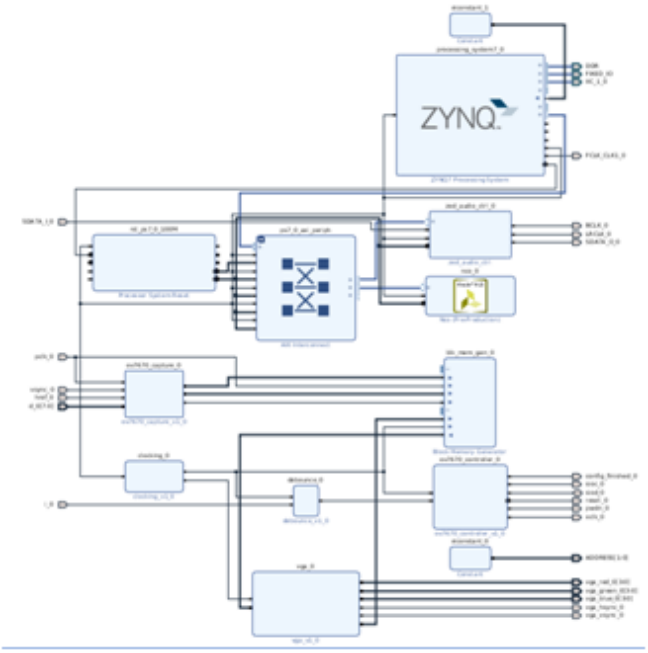


Fig.6.Block Design of embedded audio and video system

The block design is created in the Vivado and the IP blocks required for the design are added to the IP repository. In the block design, a zynq processing system is the central processing system. A processor reset IP is automatically added to the design by running block automation of the zynq processing system. Zynq processing system comprises of inbuilt memory, FCLK_RESET and wave generators. FIXED_IO, DDR, IIC and FCLK are made as external. An IP called NCO [9] from Intel is used in the design. Numerically Controlled Oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It outputs a sinusoidal waveform in two's complement representation. Another IP zed_audio_ctrl is used in the design which has different clocks BCLK, LRCLK, and SDATA_O, output of the block. Clock is used to control the encoding and decoding speed. Every IP block has slave AXI (S_AXI) inside it, and is used to connect to master AXI in the Zynq processing system. AXI_ARESET is used to reset the IP block which brings the IP core to the initialization. AXI_ General Purpose Input Output (AXI_GPIO) IP [10] block has two external

ports called leds_8bits and sws_8bits which are used to indicate the switch condition either it is in ON/OFF. Each switch generates a sin wave and is mixed with the input signal. A constant IP block [11] is used to store the present address of the ADAU1761 memory and receive data from the processor and update the address with received data.
Camera IP comprises of three components which are IIC sender, controller and registers. By configuring the registers the output of the camera is varied. As per the user requirement the internal registers are to be configured to tune the parameters like color, hue, saturation, contrast and brightness of the image. VGA IP send the data to the monitor with the help of data from D0-D7. Debounce IP is used for intialization of the camera. The captured data is stored in the Block RAM of the Zedboard and it will processed by the Zedboard. Clocking IP provides different clock frequencies required for different modules in the design.
The functionality of the hardware is defined by the Application software which was written in C language. SDK will automatically generate the drivers, Board Support Packages and debugging tool chains. The program will be transferred to the Zedboard through JTAG cable after debugging. The complete system setup is shown in the fig 7.

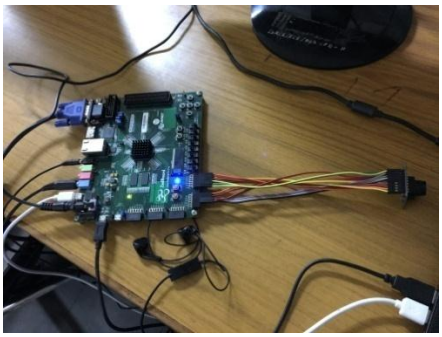


Fig.7. Hardware setup for designed audio system

VII. RESULTS

The aim of this work is providing a better solution with optimized design metrics like power, speed and area. The proposed design is implemented on Zynq-SOC which is all programmable. The following table 1 & 2 are showing that the utilization of the resources available in Zedboard. Resources include LUTRAM, Flip-Flops, Block RAM BUFGs and IOB/IO pins, for synthesis and implementation respectively. [12]. An output of the camera displayed on VGA monitor is shown in the fig 8. From the following tables it is very clear that the designed system is consuming low power, occupying less design area and gives high performance.

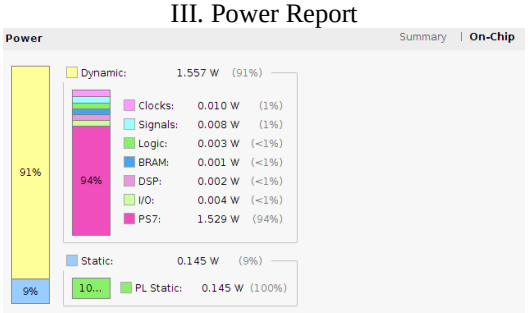
I. Utilization – Post Synthesis

Resource	Utilization	Available	Utilization %
LUT	1367	53200	2.57
LUTRAM	62	17400	0.36
FF	1302	106400	1.22
BRAM	105.50	140	75.36
IO	41	200	20.50
BUFG	6	32	18.75
MMCM	1	4	25.00

II. Timing Report

Timing	Setup | Hold | Pulse Width
Worst Negative Slack (WNS):	4.265 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4364

III. Power Report



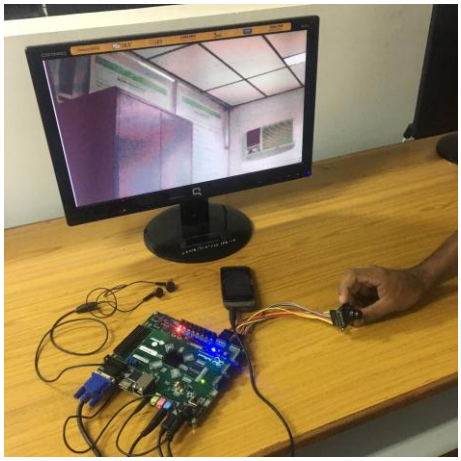


Fig 8. Output of Camera Displayed on VGA Monitor

VIII. CONCLUSION

Smart audio and video systems are used at everywhere. But, they are not handy/compact, consumes more power usually main line supply. But this smart system is occupied very less area so that it is compact/ handy. It consumes very low power but gives better performance. This system is implemented on the advance board which is a latest release from Xilinx inc. the Target hardware board is a SOC. Processor and Logic are fabricated on the same chip so that it consumes less power. The audio is fed through the microphone/line in jack. The vision is captured by the camera and displays the output at VGA monitor at 640 x 480 pixels. All the hardware designed in the Vivado is controlled by the Application software created in the SDK. The result says that the system is an optimized design.

IX. FUTURE SCOPE

The quality of audio and video is recommended by the user. The audio and video produced in this paper may contain some noise. By using digital filters, the noise can be filtered. As an extension, color filters can be used within the design.

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