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Design And Comparison Of Low Power Static RAM Using Cadence Tool In 180nm And 45nm Technology

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Abstract— In the modern technology the demand for low power gadgets has been increasing massively. The fast growth of portable battery-operated gadgets has made lower power design an important factor. In this paper, the different architectures of SRAMs are designed and the performance of each cells are tested. A comparative study is made on the delay and power dissipation. The different architectures like 6T, 7T ,8T and 9T are considered for the purpose. These cells are designed using the generic process development kit (gpdk) 180nm and 45nm technologies. The cadence-virtuoso tool is used for designing and conducting the power analysis.

Keywords— SRAM, CMOS, Cadence, Low Power, 180nm Technology, 45nm Technology

I. INTRODUCTION

It has now been a period of portable gadgets like phones, tablets, iPod and so on. A major prerequisite for all these devices is that they ought to have an extended backup for battery so that the device can be functioned for a more drawn out length with no interruption. Hence the demand and interest for memories processing in low power is high. The urge for low power consumption is increasing day by day. The memory design which is the most integral part of any device, if the power consumption for these devices are achieved then the rest parameters like system reliability, performance can be obtained.

SRAM, a memory device is used to store and access information of one bit. A bistable latching circuitry is used by the SRAM cell to store each bit. Data in static RAM (SRAM) persists for as long as power is supplied, whereas data in dynamic RAM (DRAM) must be periodically refreshed. SRAM has become an important component in CMOS VLSI chips due to their storage capacity and time of access. The SRAMs are available in different architectures. Most conventional architecture out of all is the 6T.

In this paper some SRAM cells architectures such as 6T, 7T, 8T and 9T are taken and all the architectural circuits are designed with 180nm and 45nm technologies. The performance comparison is made with the two technologies for the different architectural circuits.

II. ANALYSIS AND REVIEW OF DIFFERENT SRAM TOPOLOGIES

A. 6T Static RAM

A 6 Transistor Static RAM is the most prevailing type of cell. A 6T SRAM consists of six transistors out of which four transistors form cross coupled inverters and the other two supplementary transistors controls the access of the memory cell during the read or write operation. An SRAM cell has three modes of operation: Hold state, read and write modes.

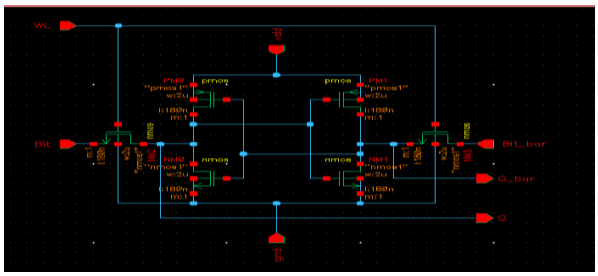

Fig 1: Schematic of 6T Static RAM in 180nm Technology.

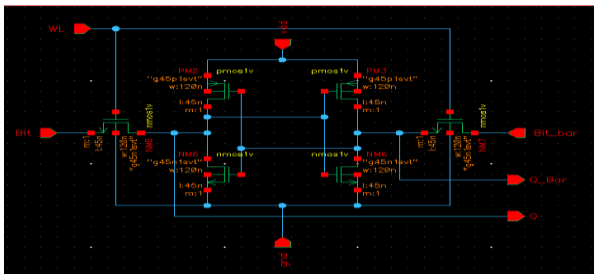

Fig 2: Schematic of 6T Static RAM in 45 nm Technology

In the course of read operation, the Bit lines are pre charged to logical 1 that is the high state and the word line is also made high. These bit lines activate the cell. The access transistors are activated when the bit lines are made high. The amplifier

will convert the signal to logical output. At the end of the operation the bitline (Bit) will discharge and the compliment Bit_bar stays high.

At the time of write operation, the word line WL is set to logical high this turns on the access transistors. The information to be stored on the cell is given through the bitlines . These bitlines stores the information in the inverters. The access transistors can be made off and the inverter will sustain the stored information.

During the hold state the circuit is considered to be ineffective. The word line is given with logical 0 in the hold state. Then the two supplementary access transistors will decouple the unit from the bitlines . In the course the two cross coupled inverters will keep on the feedback feature with each other on the condition that the power is supplied. The information is held in the unit.

The layout for the 6T SRAM in 180nm technology has been designed and is shown in fig 3. The area is calculated as 135.02µm^2.

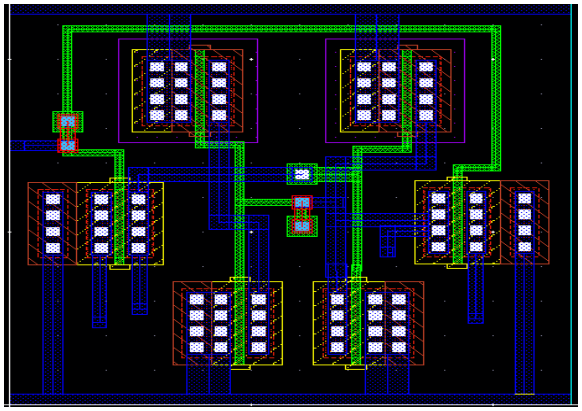

Fig 3: Layout of 6T SRAM cell in 180nm technology

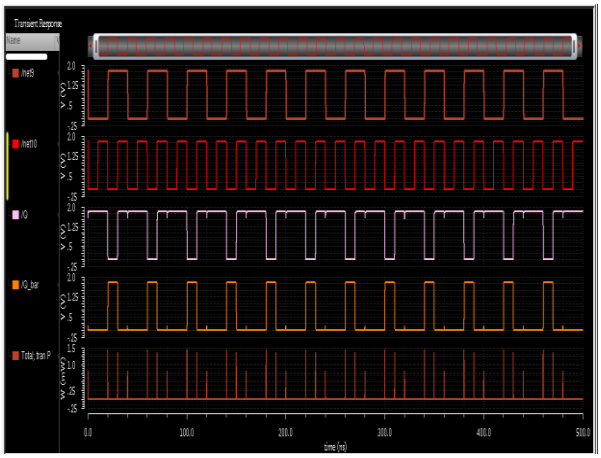

Fig 4: Output waveform of 6T static RAM in 180nm Technology

B. 7T Static RAM

A 7T SRAM consists of seven transistors, which is one extra transistor than the 6T SRAM. Four transistors form cross coupled inverters, two supplementary transistors controls the access of the memory cell during the read or write operation and the extra transistor is used as a power gate switch. The extra transistor is connected in between the ground and the cross-coupled inverter circuit.

The circuit for the 7T SRAM was implemented in 180nm technology and 45nm technology using the Cadence Tool.

The working is similar to the 6T SRAM circuit. An SRAM cell has three modes of operation, namely, hold/stand-by mode, read mode and write modes.

The gate terminal of the extra transistor is connected to the word-line input represented as WL. During the read operation, the Bit lines are pre charged and the word line is also made high. So the access transistors are activated and the cross-coupled circuit is accessed. The value stored in the cross-coupled circuit is read by sense-amplifier. The extra transistor is active during the read mode.

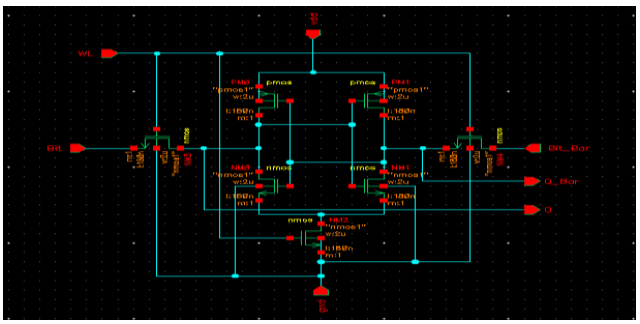

Fig 1: Schematic of 7T Static RAM in 180nm Technology.

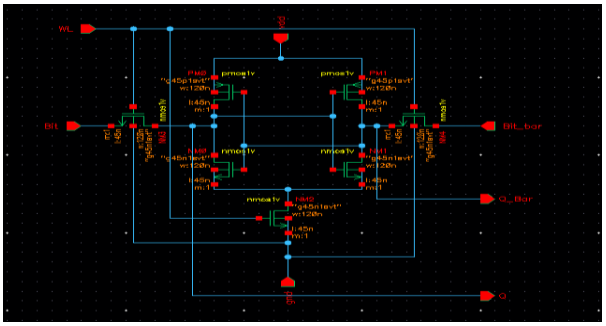

Fig 2: Schematic of 7T Static RAM in 45 nm Technology

In the write mode, the WL is made active to activate the access transistors. The value to be stored is passed through the access transistors by the bit-lines and is stored in the cross-coupled circuit. After storing the value, the WL is made low. The extra transistor is active during the write mode.

During the hold/stand-by state the circuit is considered to be ineffective. The two access transistors are made inactive by keeping the WL low and thus, the cross-coupled circuit is isolated. The extra transistor is inactive during the hold/stand-by mode as the input to the gate terminal is low. Thus, it helps to reduce the leakage power while in the hold/stand-by mode and helps to increase the data stability.

The layout for the 7T SRAM in 180nm technology has been designed and is shown in fig 7. The area was calculated as 217.039μm^2.

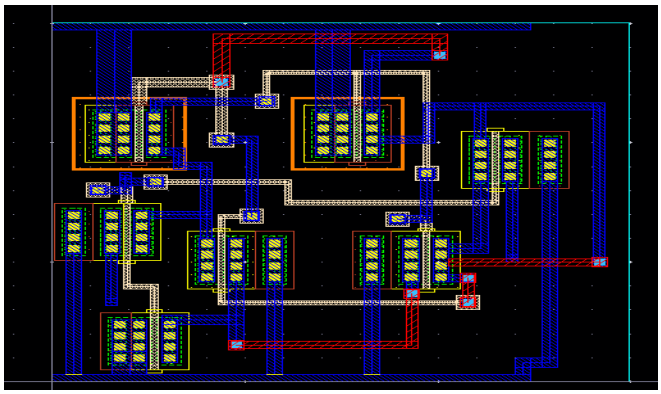

Fig 7: Layout of 7T SRAM cell in 180nm technology

C. 8T Static RAM

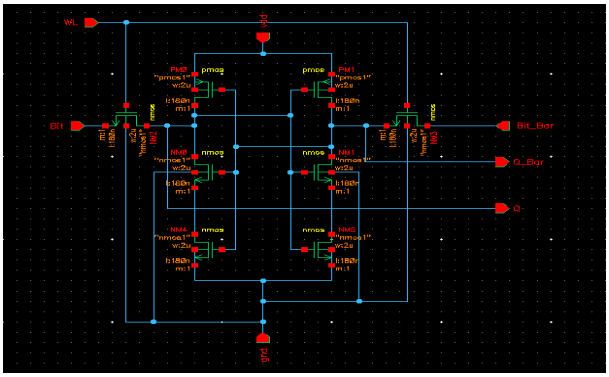

Fig 8: Schematic of 8T Static RAM in 180nm technology

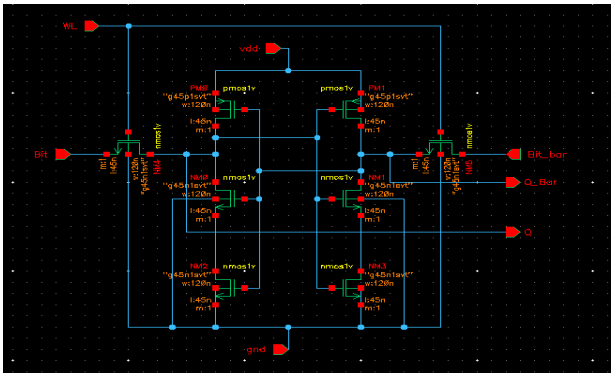

Fig 9: Schematic of 8T Static RAM in 45nm technology

The 8T SRAM is made up of eight transistors out of which the six transistors M1 to M6 form the traditional6T SRAM and the transistors M7 and M8 form the additional transistors. To write a logic 0, the bit line Bit is made low and to write logic 1 the bit line Bit is made high. Read cycle starts by precharging both the bit lines Bit and Bit_bar to logic 1. Since the additional transistors of the conventional 8T SRAM does not contribute in the process of power consumption, the

power consumed by the 8T SRAM is more when compared with the conventional 6T, 7T and 9T SRAM. Even though the 8T SRAM consumes more power than the 6T SRAM, 8T SRAM is considered to be more stable than the 6T SRAM. The layout for the 8T SRAM in 180nm technology has been designed and is shown in fig 10. The area was calculated as 255.2385 μm^2.

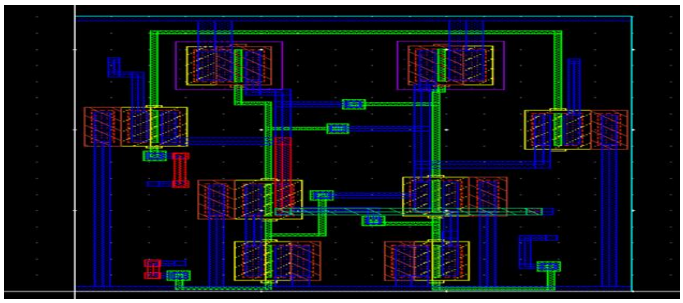

Fig 10: Layout of 8T SRAM cell in 180nm technology

D. 9T Static RAM

9T SRAM is designed by adding three additional transistors to the conventional 6T Static RAM architecture. These three additional transistors have the advantage of bypassing the read current. Read current is bypassed from the node known as data storage. 9T SRAM consists of two sub circuits referred as upper sub circuit and lower sub circuit. Sub circuit in the upper part of the 9T SRAM architecture is composed of 6T SRAM cell. Sub circuit in the lower part composed of the transistors which are utilized for accessing the bit lines and read. Upper memory sub circuit is utilized for storing the data. Data put away inside the Static RAM cell used to control the functioning of the cell. Write signal is employed to control the transistors that are used for accessing the write signal.

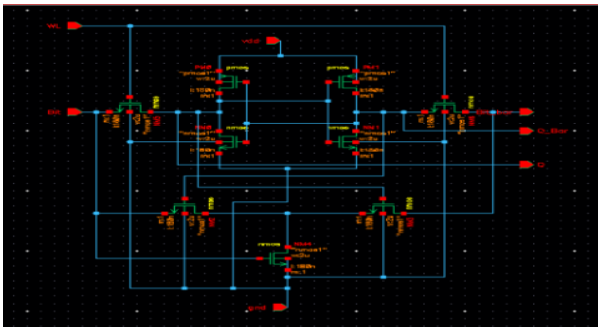

Fig 11: Schematic of 9T Static RAM in 180nm Technology

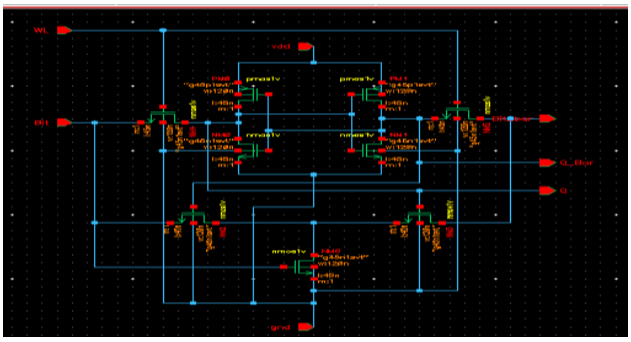

Fig 12: Schematic of 9T Static RAM in 45nm Technology

To start off the write performance WL = 1 and RD = 0. Transistors M1 and M2 will have the value 1 during the write action. Value in transistors M8 and M9 changes whenever there is a change in transistor M7. To start off the read performance WL=1 and RD=1. Read action leads M7 in the saturation mode. Isolation of the Data takes place from the bit lines during the read action. Also, in the course of read action cell will be highly stable. 9T SRAM cell is set to a sleep mode known as super cut-off to lower the consumption of leakage power.

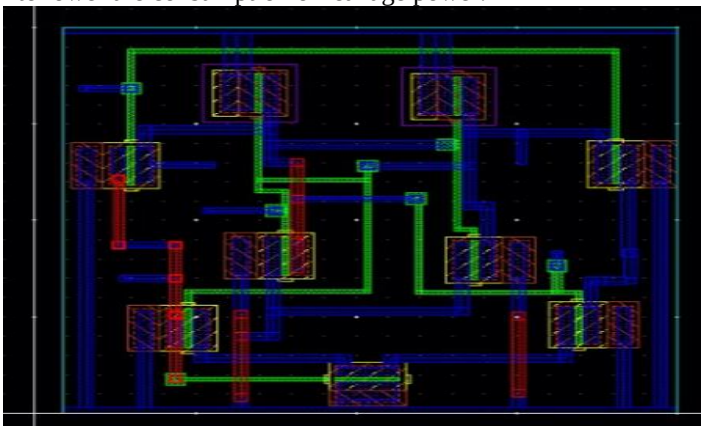

Fig 13: Layout of 9T SRAM implementation for 180nm technology

The layout for the 9T SRAM in 180nm technology has been designed and is shown in fig 13. The area was calculated as 382.8 μm^2.

III. RESULTS

TABLE I

The comparison of power and delay obtained after implementing the 6T, 7T, 8T and 9T SRAM architectures in 180nm and 45 nm technologies.

Parameters	180nm				45nm			
	6T	7T	8T	9T	6T	7T	8T	9T
Transient Power(W)	1.42m	7.74µ	8.9µ	13.05µ	223.03µ	787.2n	846.4n	1.34µ
DC Power(W)	2.01m	2.01m	2.004m	2.688m	320.7µ	318.7µ	316.5µ	393.7µ
Delay(Rise to Fall)	74.3ps	71.3ps	80.88ps	78.56ps	78.55ps	71.3ps	74.06ps	79.4ps
Delay(Fall to Rise)	29.98ns	29.98ns	29.99ns	29.99ns	29.95ns	29.94ns	29.9ns	29.9n

TABLE II

The comparison of area obtained after implementing the 6T, 7T, 8T and 9T SRAM architectures in 180nm technology.

Parameter	180nm in (μm^2)			
	6T	7T	8T	9T
Area	135.02	217.039	255.2385	382.8

IV. CONCLUSIONS

The different SRAM cells of 6T,7T,8T and 9T have been designed. The operation of variant SRAM architectures is studied and analysed. The various architectures are implemented in 180nm and 45nm technology using cadence tool. The parameters like power, delay and area is calculated. The obtained values are compared within the two technologies. The traditional 6T SRAM has the least number of transistors but the power consumption is very high. The 9T SRAM architecture shows enhanced data stability and it consumes less power.

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